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The Capacitive Division Image Readout; An imaging technique combining high time and spatial resolution

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Presentation Overview

- INTRODUCTION....system overview
- DESIGN, SIMULATION AND MANUFACTURE....of C-DIR
- EXPERIMENTS AND RESULTS....for C-DIR
- CONCLUSIONS

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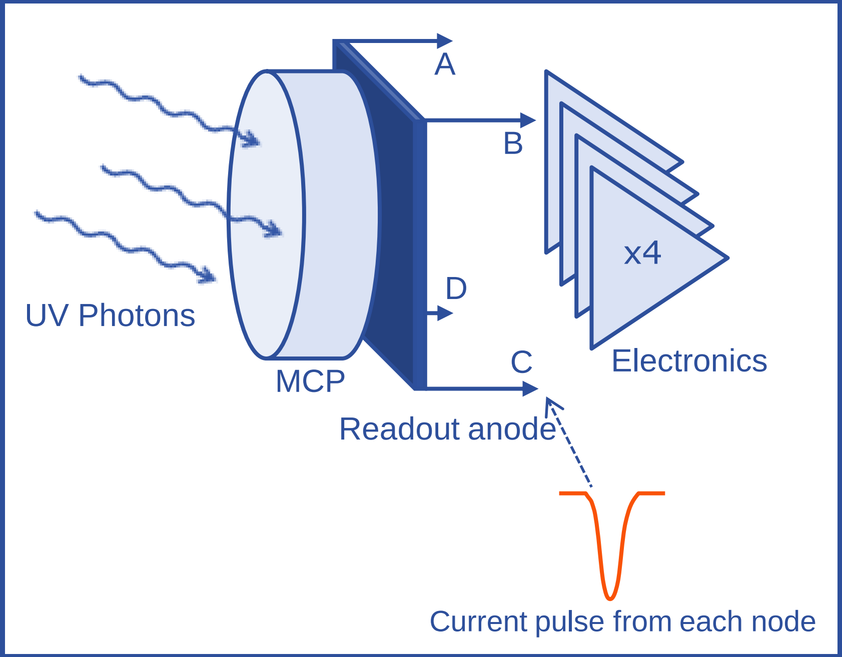
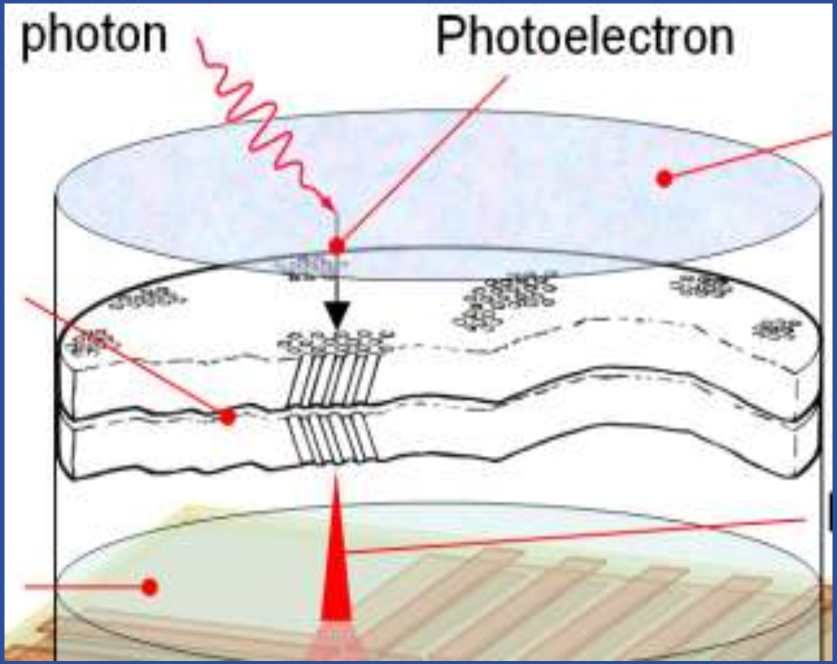
INTRODUCTION

System overview: MCP detector, readout & analogue electronics.





Electron cascade through Microchannel Plate and electron cloud incident on readout anode for measurement.

MCP stack run in high gain, saturated, mode. $>10^6$ electrons.

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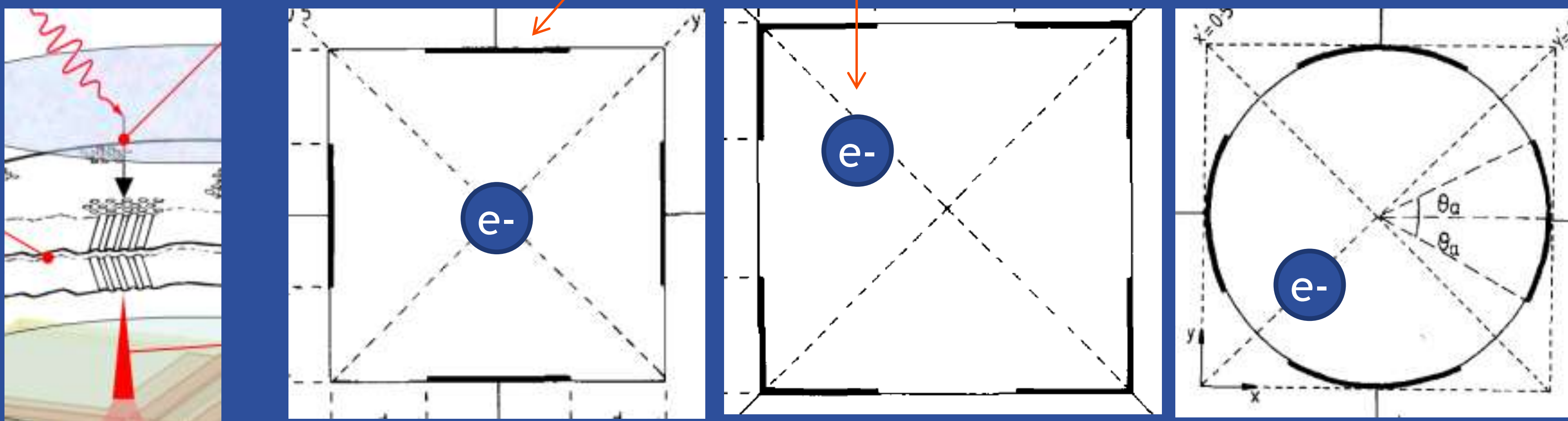
INTRODUCTION

$$x = \frac{(A+D)}{(A+B+C+D)}, \quad y = \frac{(A+B)}{(A+B+C+D)}$$

Charge division - Charge centroid centre of gravity encodes the 2-D coordinate of the event. Dividing charge among a small number of instrumented nodes. Charge amplitudes are measured and an algorithm used to decode event position coordinate.



Fraser (1980&81)

Several methods can be used to divide the charge amongst the measurement nodes:

- Resistive
- Geometric
- Capacitive division

INTRODUCTION: Resistive division

- Resistive anode, popular technique.

- Event charge cloud collected on resistive sheet ~10 kΩ to 1 MΩ per square.

- Charge resistively divided amongst four perimeter contacts, electronically measured and event coordinate calculated using an algorithm such as:

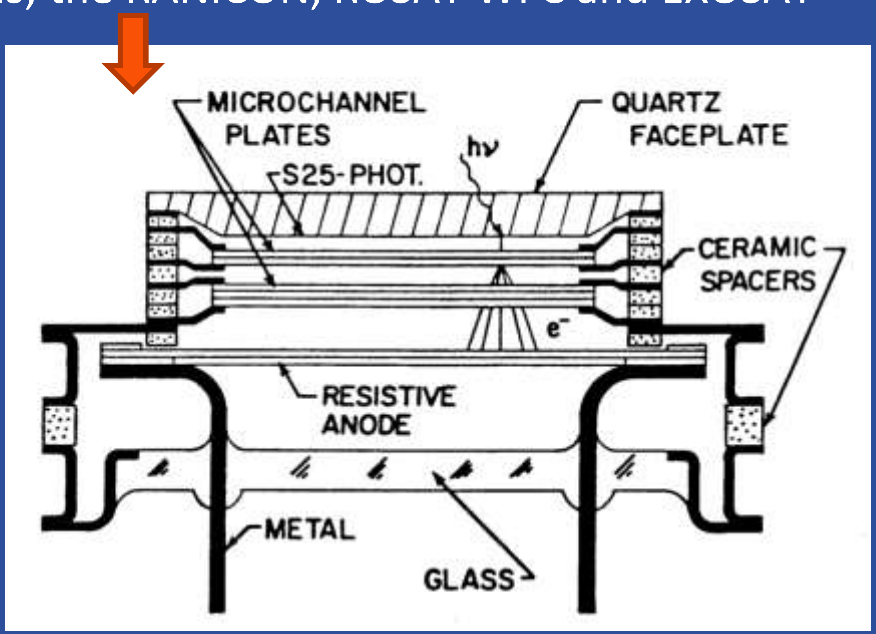
$$x = \frac{Q_A + Q_B}{Q_A + Q_B + Q_C + Q_D} \qquad y = \frac{Q_B + Q_C}{Q_A + Q_B + Q_C + Q_D}$$

- Ground based and space based applications; the RANICON, ROSAT WFC and EXOSAT

- Resolution dominated by two noise components; resistive thermal noise or 'Johnson' noise & pre-amplifier noise.

➢ Limits resolution to several tens of µm.

➢Timing restricted (RC).



Lampton (1974)

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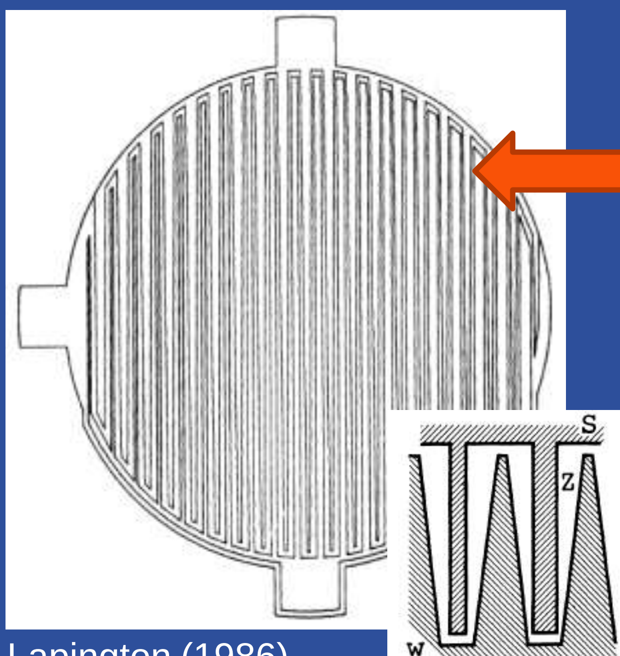
INTRODUCTION: Geometric division

- E.g. wedge and strip anode (WSA). Small number of interleaved conductive electrodes to collect the charge. Modulation of the electrode areas to charge ratio.

- Inherently faster than resistive (conductive electrodes).

- Interleaved nature can cause a) higher electrode resistance b) high inter-electrode capacitance (more noise) c) dynamic image drifts due to redistribution of SE.



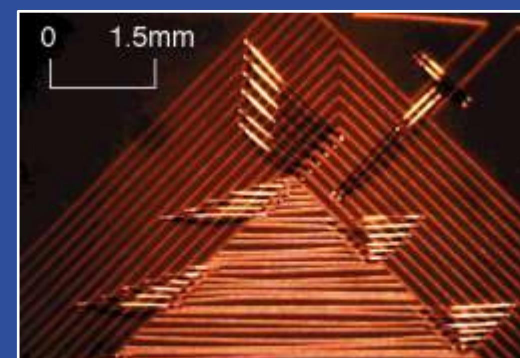
Lapington (1986)

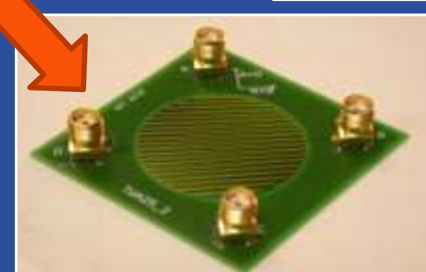
$$X = \frac{2Q_S}{Q_W + Q_S + Q_Z}$$

$$Y = \frac{2Q_W}{Q_W + Q_S + Q_Z}$$

Examples:

- Wedge Strip Anode
- Vernier Anode
- Tetra Wedge Anode





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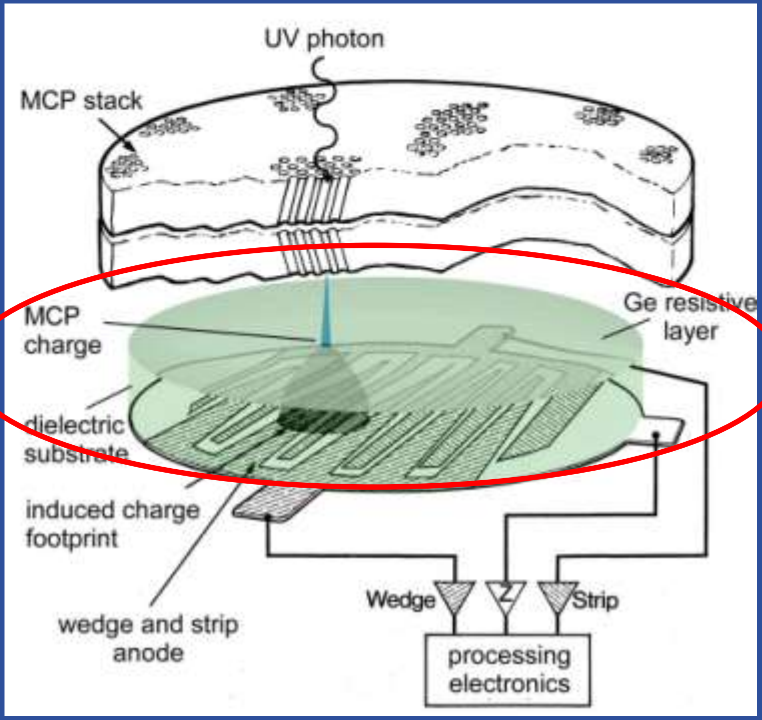
INTRODUCTION:
A note on Image Charge.........

- Charge cloud is collected on a passive resistive anode coupled to a conductive readout such as a WSA via a dielectric substrate.
- Resistive layer physically localises the charge while the readout detects the signal transient induced through the dielectric.
- Signal charge slowly leaks away through the resistive layer.
- Removes SE redistribution, constant charge footprint, avoids the partition noise.
- Allows readout to be operated at ground irrespective of the detector anode voltage.



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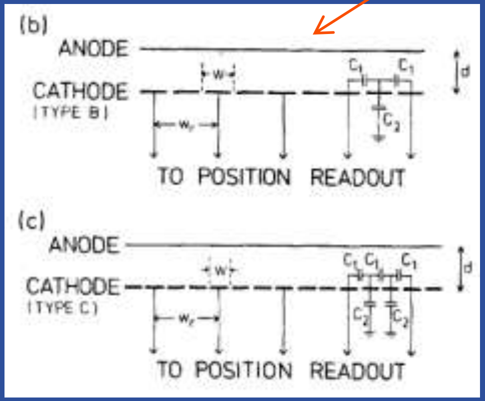
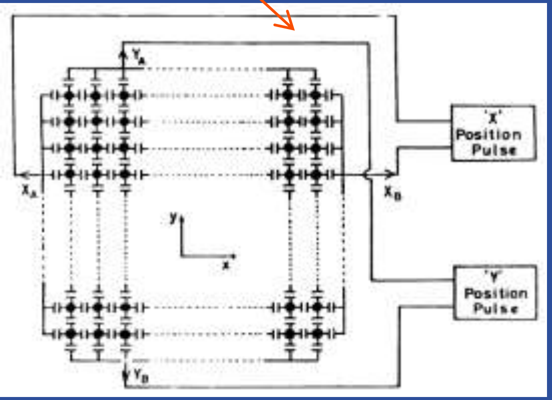
INTRODUCTION: Capacitive division

- Capacitive division experimentally demonstrated before. Gott(1970); 2-D square array via wires to an separate capacitor network . Smith(1988); array of 1-D strip electrodes to charge share. Drawbacks; discrete capacitors, parasitic capacitance, bulky, engineering complexity.

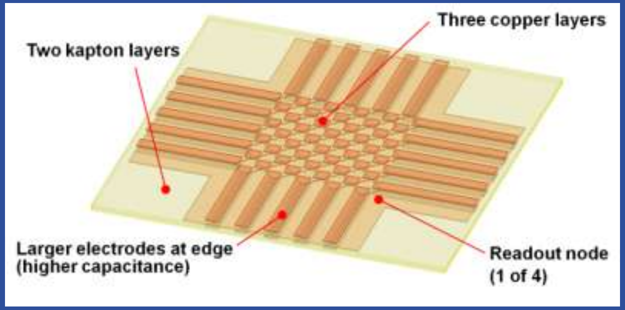




Development of a capacitive division readout:

Capacitive Division Image Readout (C-DIR)

- 2-D array of isolated electrodes which divide the signal via their mutual capacitance to four measurement nodes at four corners of the readout.



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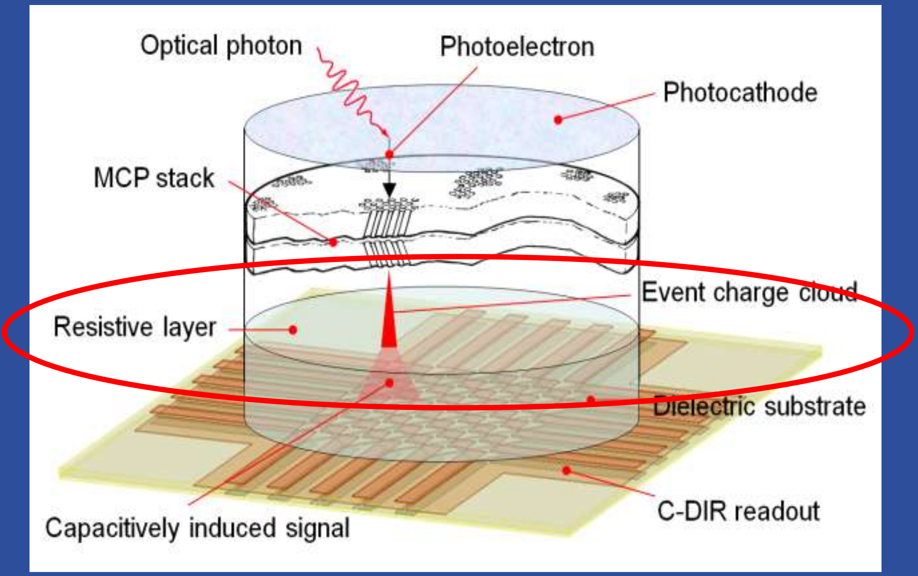
DESIGN, SIMULATION AND MANUFACTURE: C-DIR



Stage 1: Resistive Anode

- Charge collected by the resistive anode (electrodes do not need to be resistively coupled).
- Resistive layer localizes charge, signal transient couples through dielectric.

- RC time constant has no influence on the transient signal.
- SE redistribution of the primary event charge occurs but its footprint is symmetric, stable and predictable.

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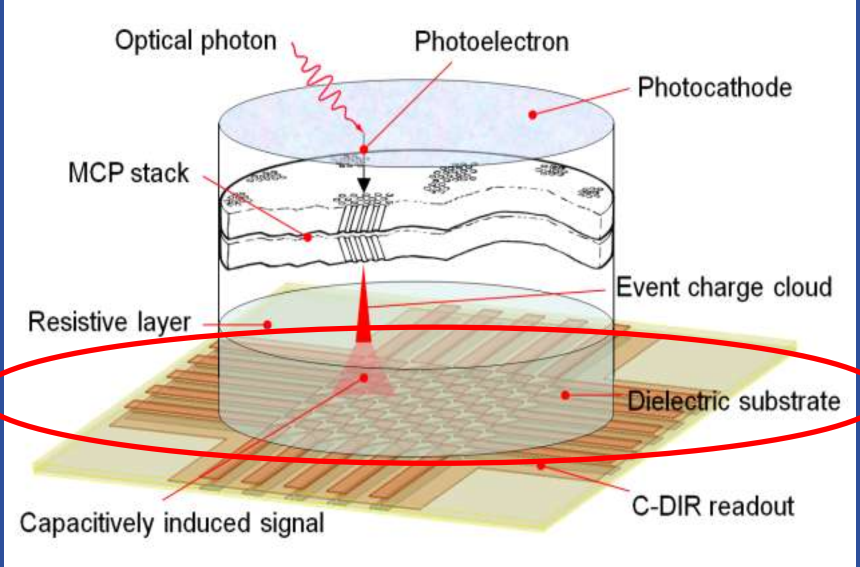
DESIGN, SIMULATION AND MANUFACTURE: C-DIR

Stage 2: Dielectric Substrate

- Alumina dielectric layer (typ. 2 mm thick) supports the RA (thickness defines footprint).
- Stands off detector high voltage.

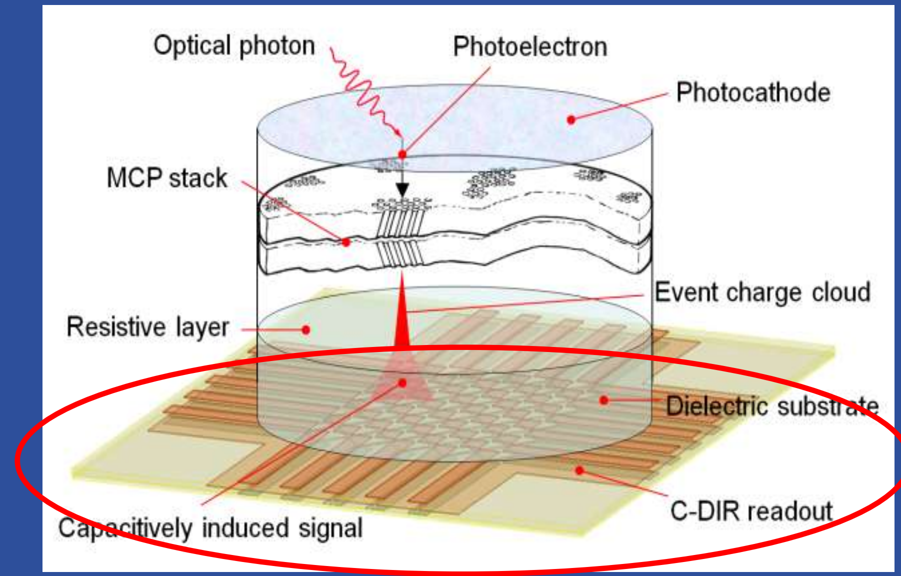


- Acts as the rear vacuum vessel wall, readout completely outside the vacuum environment, no feedthroughs required.
- Only resistive layer connection, through perimeter via its metallic support flange.

DESIGN, SIMULATION AND MANUFACTURE: C-DIR

Stage 3: Readout

- Simple passive, multilayer PCB
- Matrix of isolated electrodes, geometry defines the mutual capacitances.
- Signal charge induced is capacitively shared among the four charge measurement nodes.



- Intrinsic capacitance array minimizes parasitic capacitance, <noise, >resolution.
- Minimize dominant parasitic capacitance (MCP output face) to <10% by detector geometry and dielectric choice.
- Array capacitance small => preamplifier input load <5 pF (25 mm^2) (cf. 40-70 pF comparable WSA).
- Capacitive signal chain: Very high bandwidth, extract position & event time resolution in the sub-100 ps range.
- ......more

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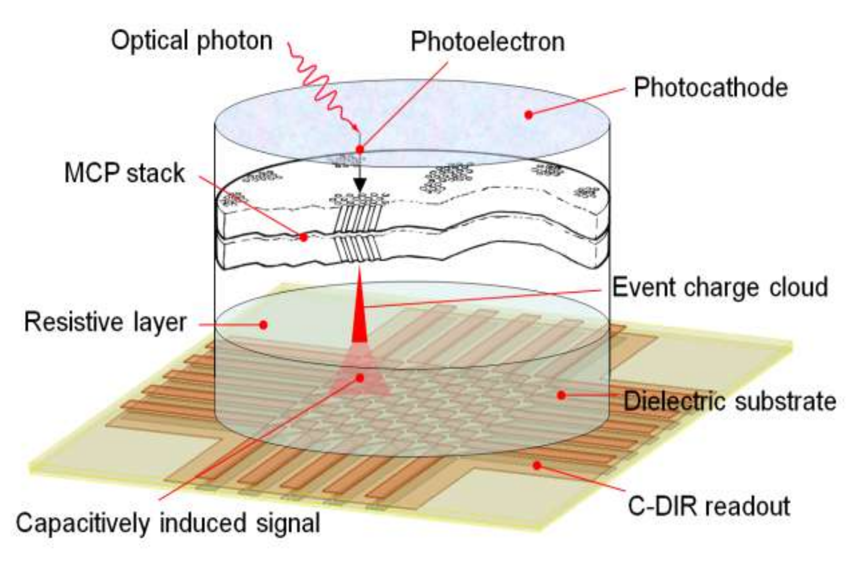
DESIGN, SIMULATION AND MANUFACTURE: C-DIR

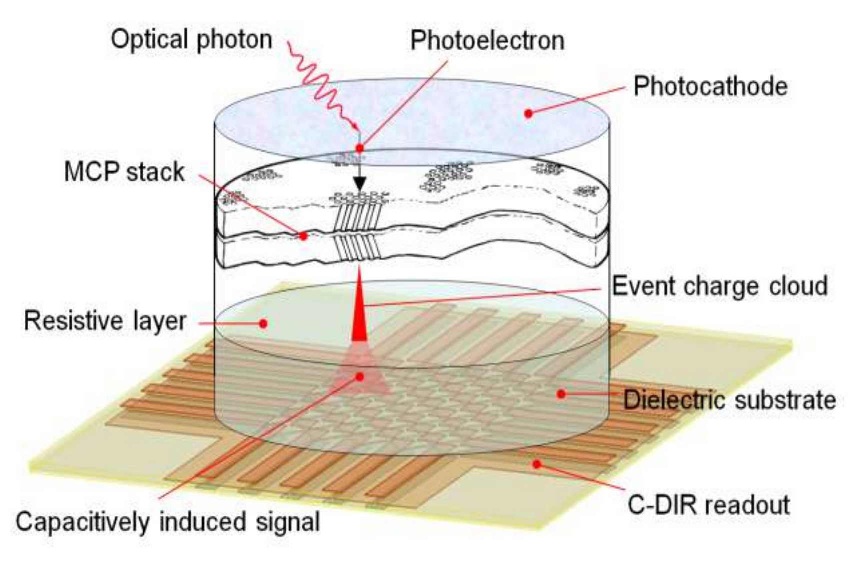
...Stage 3 cont: Readout

- Exploits full dynamic range of all 4 electrodes (cf. WSA <33% of the signal).
- Predictability of footprint distribution allows precision optimization of readout electrode array pitch and linearity control.



- Outside the vacuum (hermetically sealed from sensitive internals) => readout requires standard PCB materials and manufacturing techniques => low risk and economical.

DESIGN, SIMULATION AND MANUFACTURE: C-DIR



Overall

- C-DIR components manufactured using robust, well characterized, radiation-hard materials.

Manufacture

- Resistive layer; thick film screen printing technology.
- Robust alumina dielectric substrate.
- Conventional PCB readout.
- C-DIR; simple surface contact with the rear face of the alumina dielectric.

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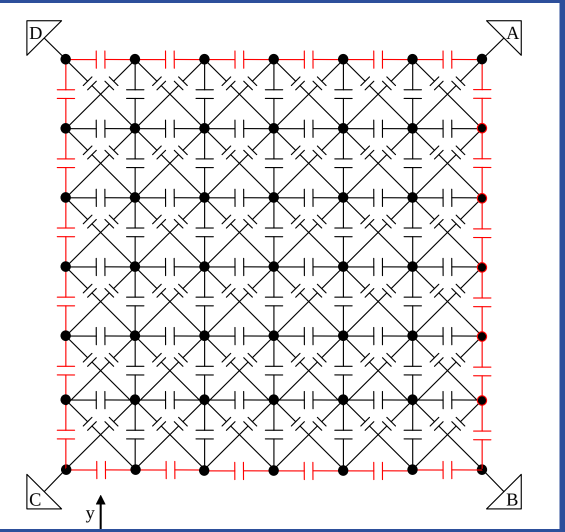
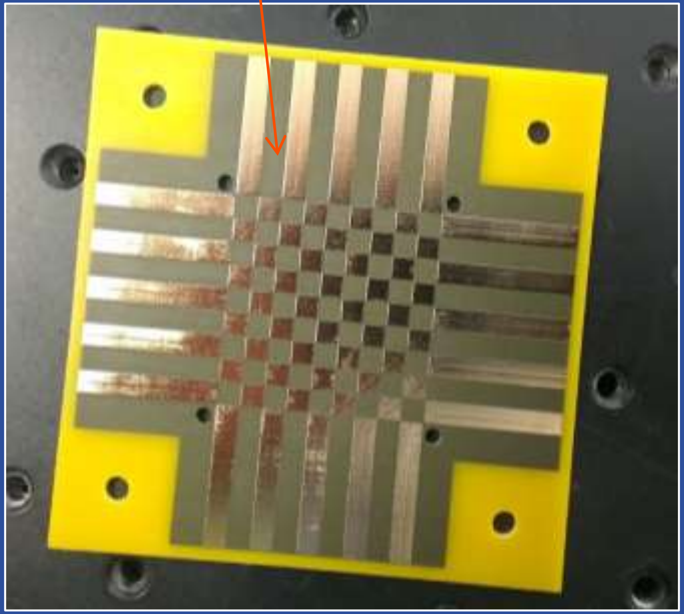
DESIGN, SIMULATION AND MANUFACTURE: C-DIR

- Original design analogous to resistive anode; uniform low value capacitive coupling surrounded by perimeter of higher capacitance (for linearity) achieved by modulating the area of the perimeter electrodes.





- Optimized 25 mm active area C-DIR.
- Comprises three layers of isolated conductors separated by thin insulator.
- Overlap between conductors on adjacent layers defines the mutual capacitances.
- Only 10 pattern pitches (2.54 mm); sharing of the induced signal between multiple electrodes => centroid footprint.

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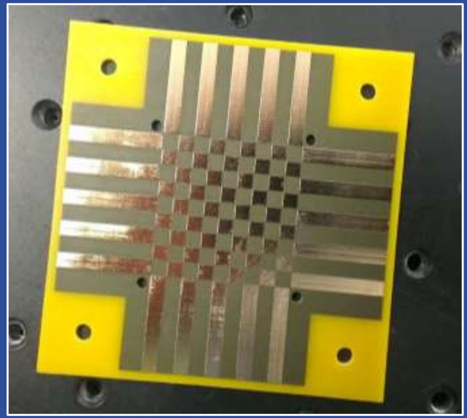
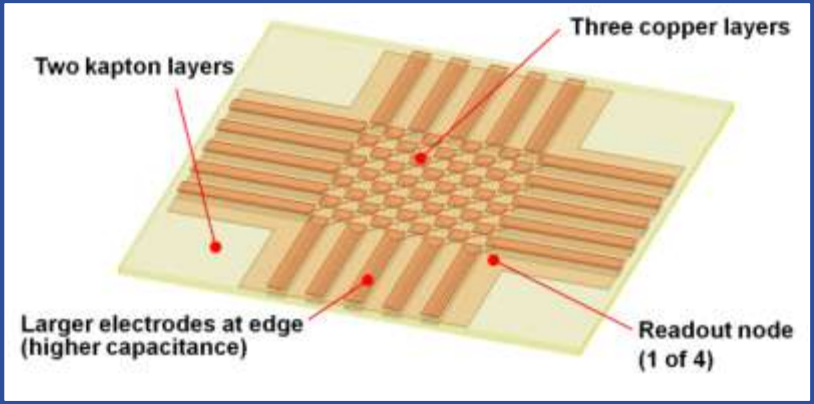
DESIGN, SIMULATION AND MANUFACTURE: C-DIR

Advantage summary:

- Capacitive nature avoids partition noise (physical collection of quantized charge carriers).
- Avoids serial resistive noise.
- DC signal discharge current (resistive anode) has no influence on the readout signal timescales.
- Dominant remaining noise; capacitive load on each preamplifier is very low.
- Pattern-edge geometry optimization => ~90% linear dynamic range.
- Resulting spatial resolution >2000 x 2000 pixel^2 (using ultra low noise electronics).





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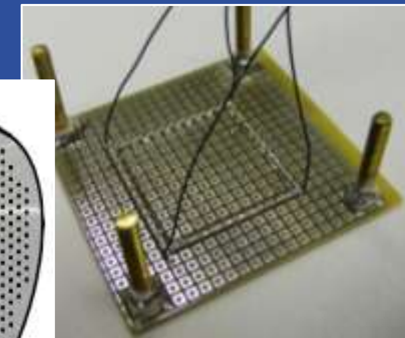
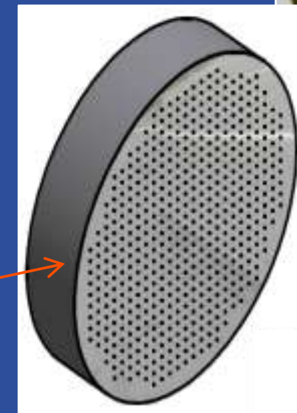
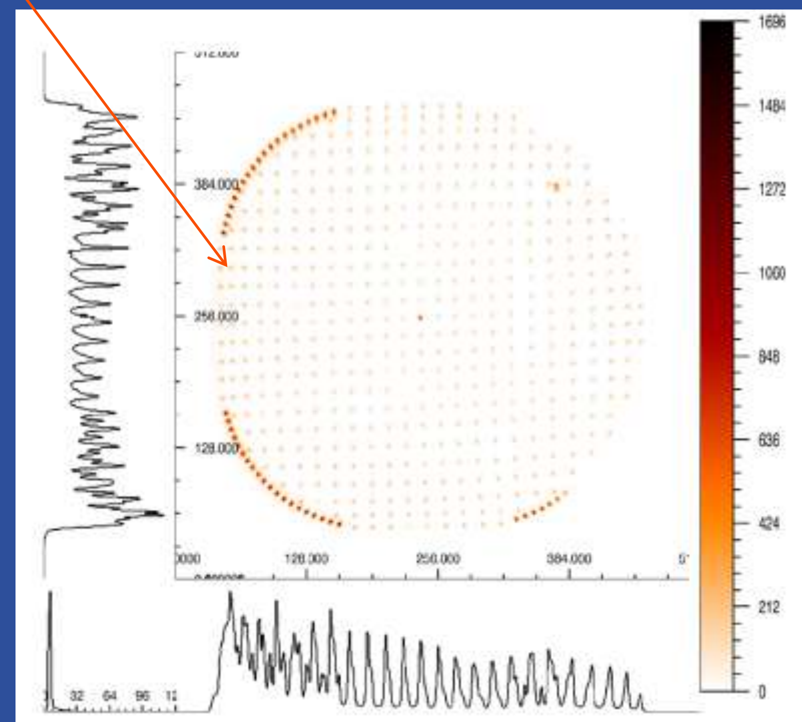
EXPERIMENTS AND RESULTS

- Prototype C-DIR device; PCB, double-sided array of conductive square pads, 2.54 mm pitch.
- Pinhole array mask image (25 µm & central 50 µm diameter pinholes).
- Spatial resolution 150 µm FWHM @ ~10^6 electrons.
- Proved concept, measured performance limited:
  - Signal loss to the rear MCP contact by parasitic capacitance.
  - Coaxial cable to the CSP =>dominant capacitive load.
  - Optical broadening of image on detector PC (source collimation and diffraction).







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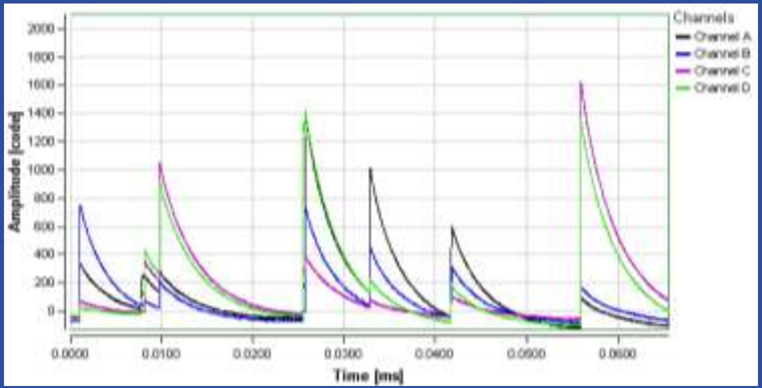
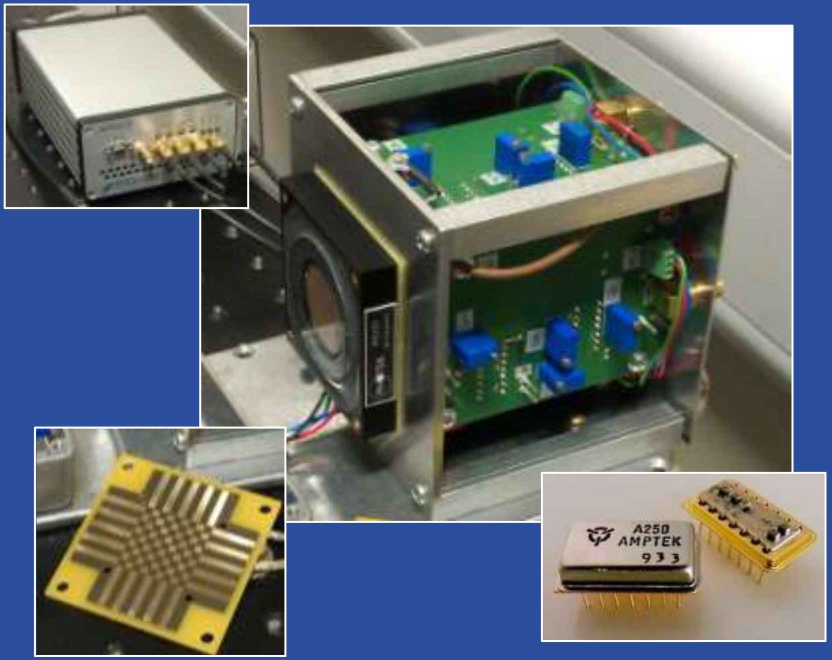
EXPERIMENTS AND RESULTS: Adaptive electronics

- Investigated variety of configurations of charge measurement electronics.
- Can utilise traditional pulse processing designs (resistive anode, WAS anode, etc.).
- Exploit extended spatial resolution/maximum-count-rate envelope:
  - Use high speed digitisation & adaptive digital filtering (req. ESA JUICE mission).
  - Trade-off between overall count rate and spatial resolution to be dynamically selected to suit science requirements.

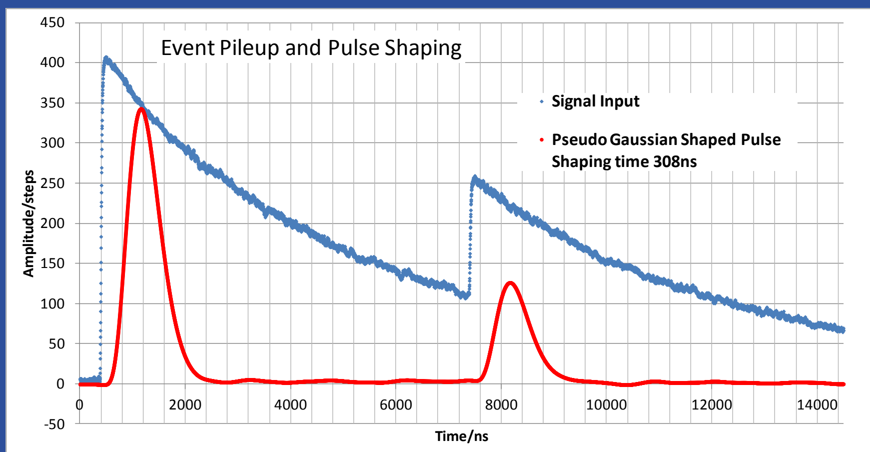
- Developed demo laboratory system:
  - C-DIR & MCP close-coupled.
  - Amptek A250 & A275 optimised for high rate or high spatial resolution imaging.

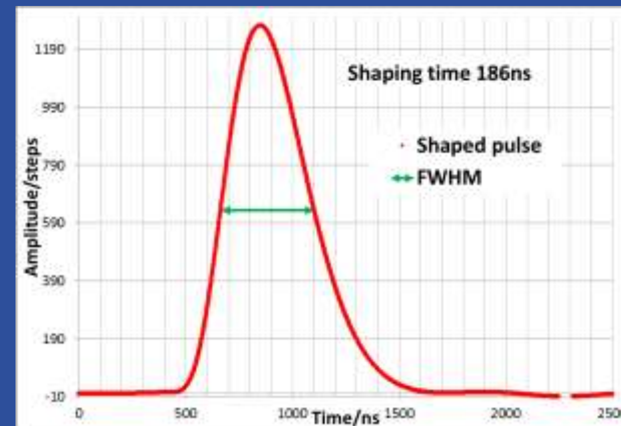


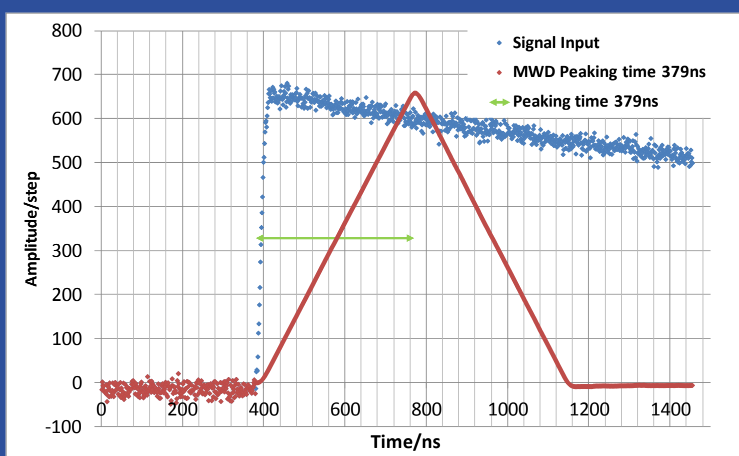


EXPERIMENTS AND RESULTS: Adaptive pulse shaping

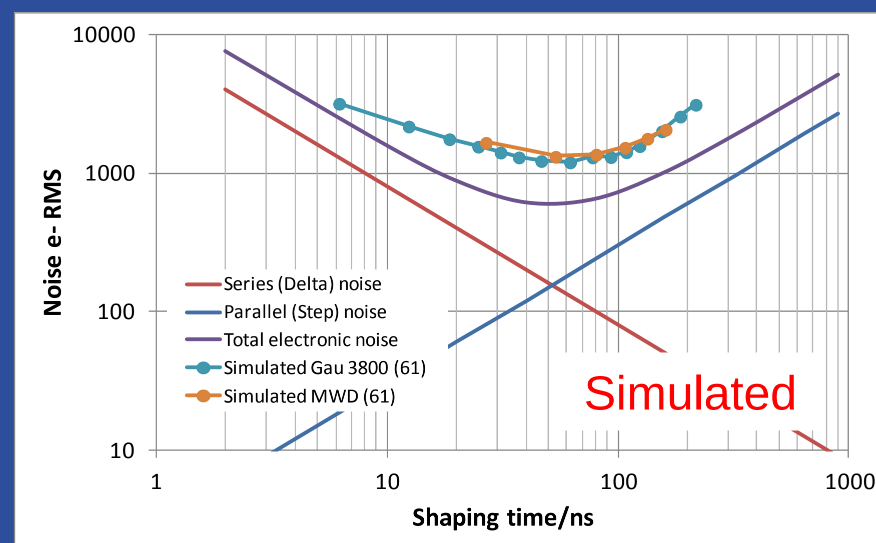
- Investigating various filtering schemes digitally encoded (Moving Window Deconvolution , pseudo Gaussian, CR-RC^n). Adaptability to count rate.





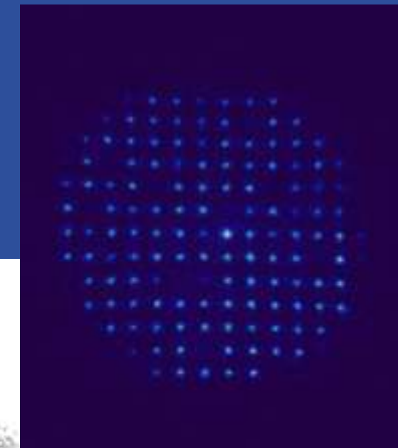


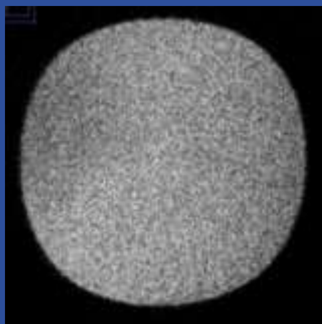
MWD

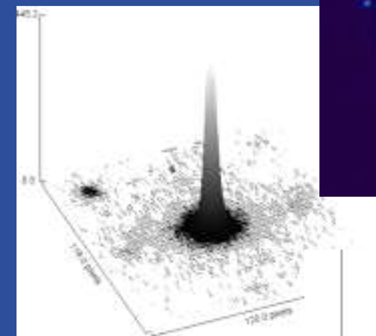


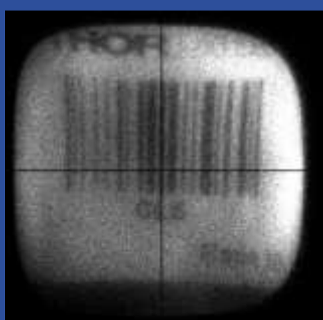
EXPERIMENTS AND RESULTS:

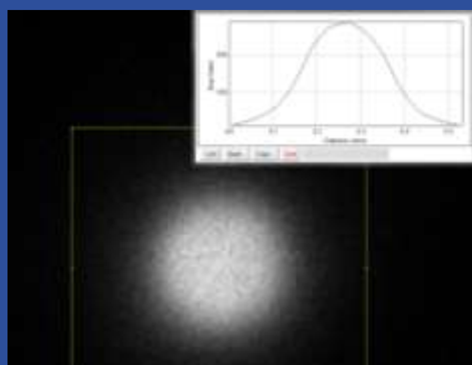
- First imaging results: Aperture, pinhole & array, slit, diffraction and various other photon counting test images.

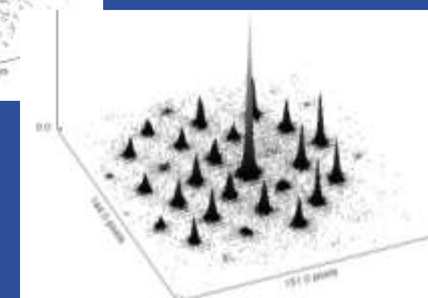


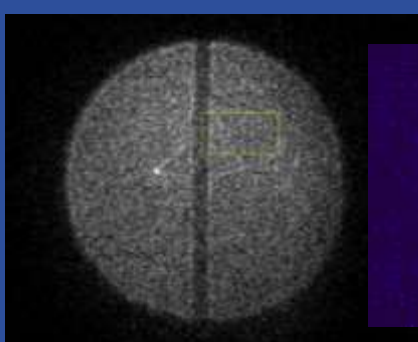


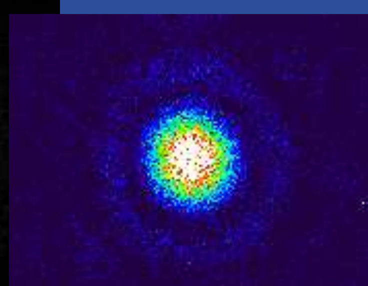


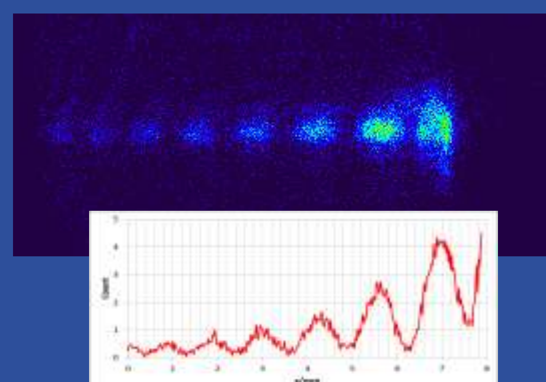


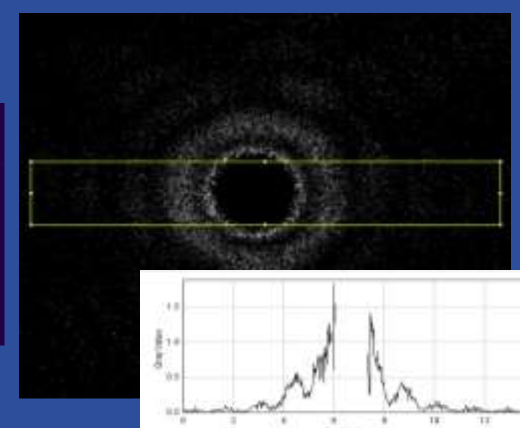












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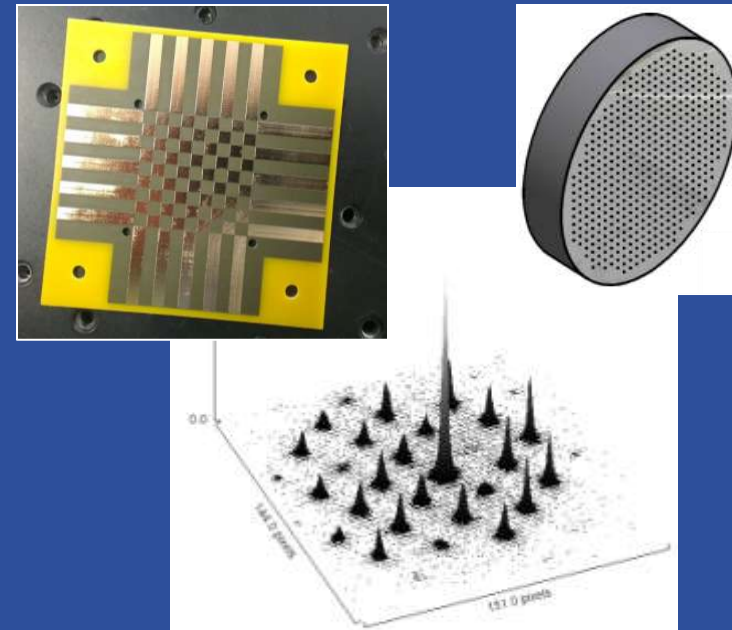
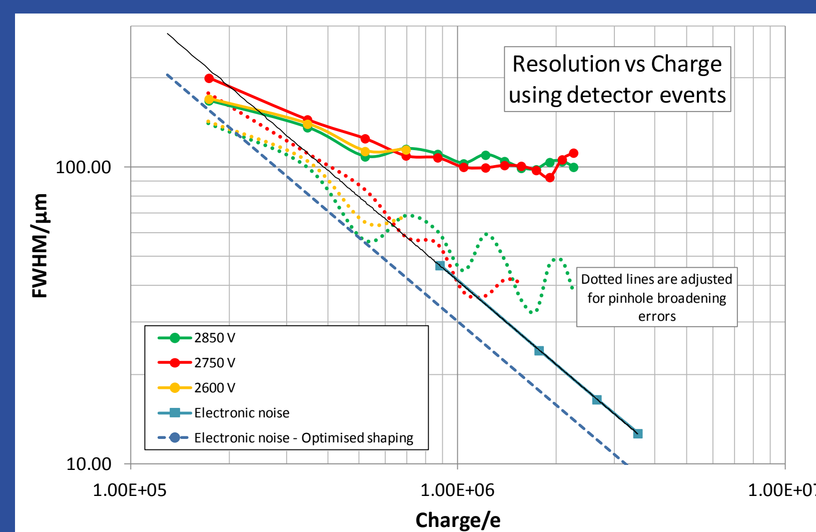
EXPERIMENTS AND RESULTS:

- Optimised 25 mm C-DIR design.
- Collimated light source to pinhole array mask on detector (25 µm & central 50 µm pinholes).
- Measured electronic noise & detector resolution.



Measured electronic noise equates to 7.7 µm at 4.3 x 10^6 electrons

- Measured pinhole width image controlled by:
  - 50 µm diameter of the pinhole.
  - Collimator pinhole in front of the LED source.
  - Distance of the mask from PC (window thickness).
  - Diffraction (mask pinhole size at the LED λ).
  - Proximity focus broadening PC & MCP.
  - Centroiding errors within the MCP stack.
  - Electronic noise (CME).



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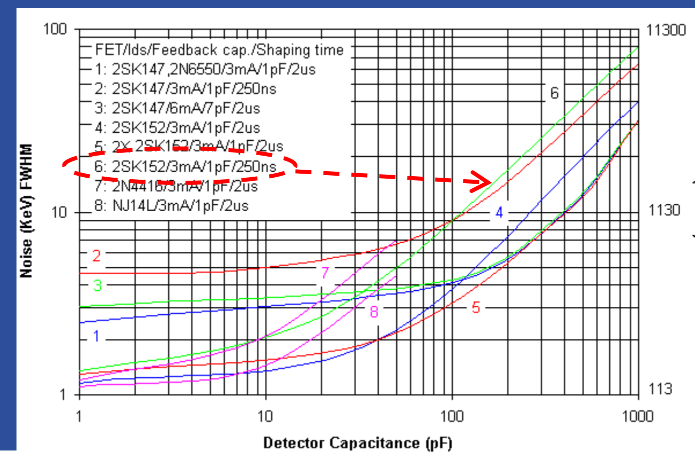
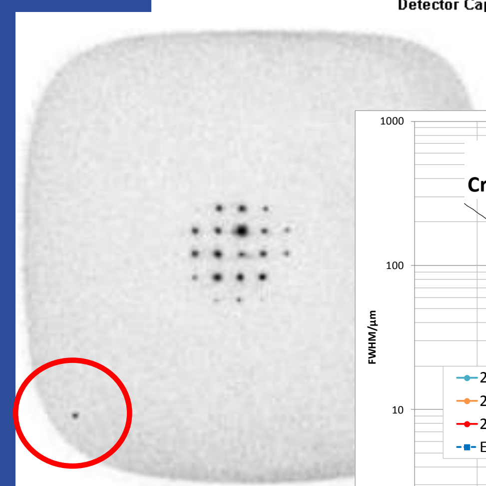
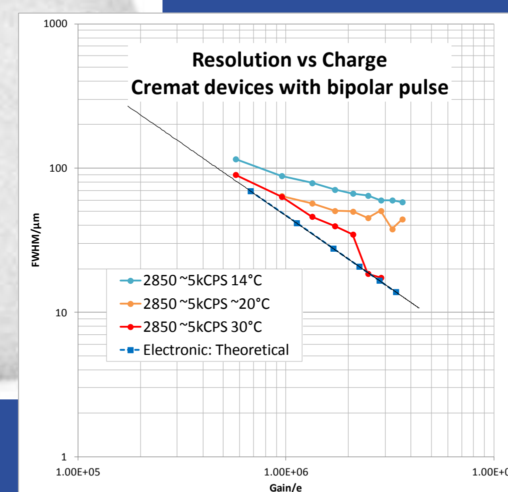
EXPERIMENTS AND RESULTS:

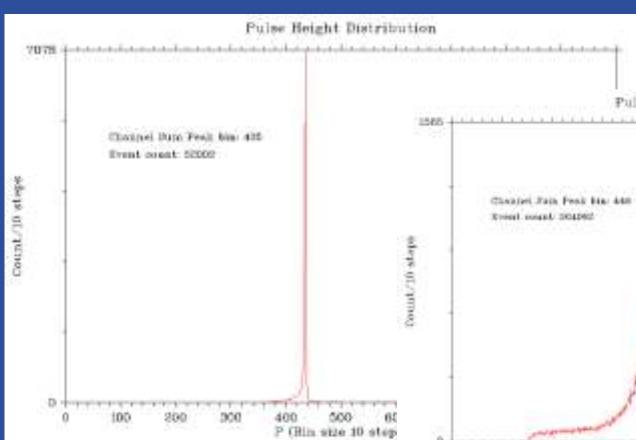
Measured electronic noise equates to 7.7 µm at 4.3 x 10^6 electrons.

- Translating into spatial resolution is proving challenging:
  - Low noise amplifiers difficult to reproduce manufacturers specification of 200 e^-RMS
  - Hot spot on sealed tube MCP causing high background limiting signal
  - Temperature response of MCP plates
  - Optical path influences
  - Unipolar signal increasing pulse pileup









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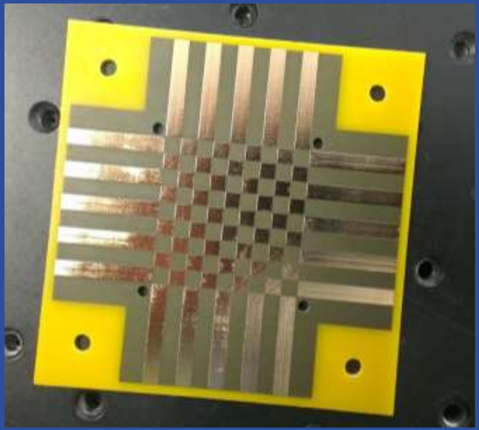
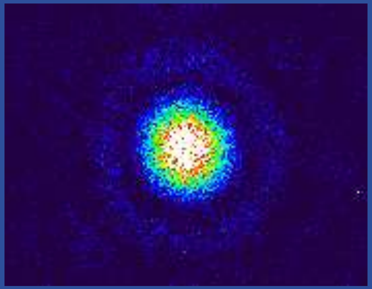
CONCLUSIONS

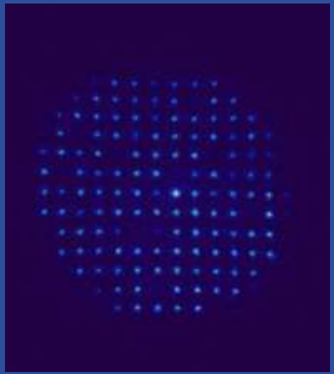
C-DIR: Capacitive Division Image Readout



- Device is a simple, low cost, easily manufactured.
- Centroiding readout device, only four electronic channels.
- Offers significant performance and operational advantages.
- Imaging performance dominated by electronic noise.
- Low capacitive load, potential resolution of 10 µm FWHM at a gain of ~ 3×10^6 electrons.
- Combined imaging and event timing sub 100 ps, close to the limit of the MCP itself.

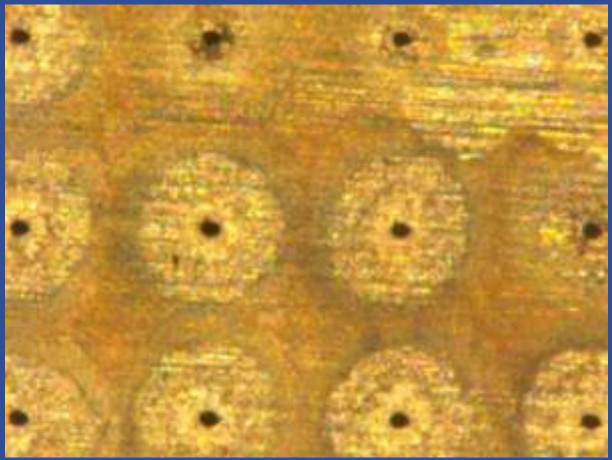


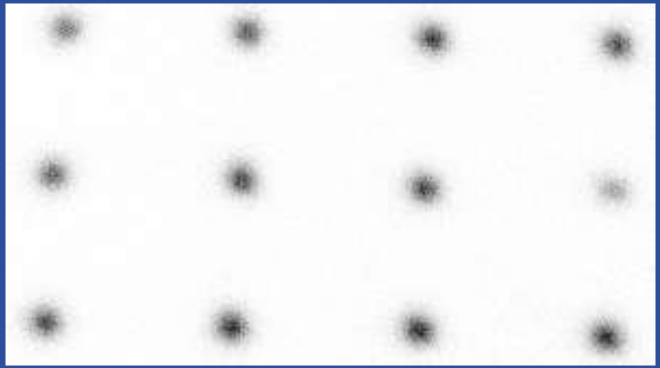
Thank you for listening
Contact: Steven Leach, sal41@le.ac.uk
www.physicsresearch.co.uk



FUTURE IMPROVEMENTS:

- Re-visiting grounding plate of FEE circuit
- Use new bare MCP in vacuum chamber
- Use direct UV, no PC focussing issue
- Expand dynamic range of FEE
- Optimise shaping time
- Rev2 to linearise C-DIR





REFERENCES

Thank you for listening.

Presenter: Steven Leach

Space Research Centre, University of Leicester, UK

For references please see:

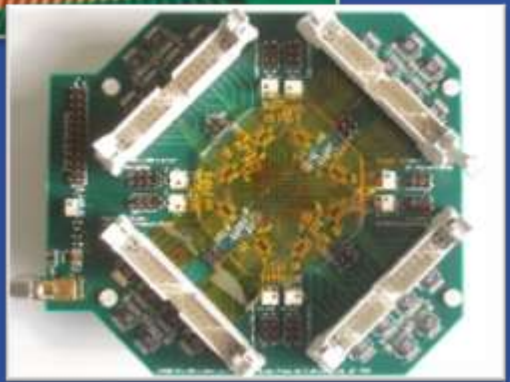
The Capacitive Division Image Readout: A Novel Imaging Device for

Microchannel Plate Detectors: Lapington NDIP 2014 8859 - 32.

EXPERIMENTS: High speed electronics

Another electronic approach:

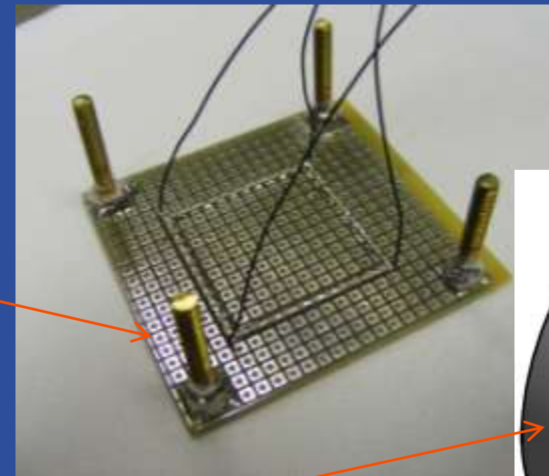
- Exploit ~30 ps event timing of MCP (purely capacitive design, no resistive elements in signal path) => nanosecond shaping times.
- High speed charge measurement => imaging & sub-100 ps event time resolution.
- Count rate capability in the 10 MHz range.
- Applications requiring fast event timing (wide-field fluorescent lifetime imaging) .
- Multi-channel NINO amplifier/discriminator ASIC developed at CERN for the ALICE time-of-flight subsystem.
- High Performance Time to Digital Convertor (HPTDC) ASIC (CERN).
- Combined uses time-over-threshold (TOT) technique for event timing correction =>25 ps.

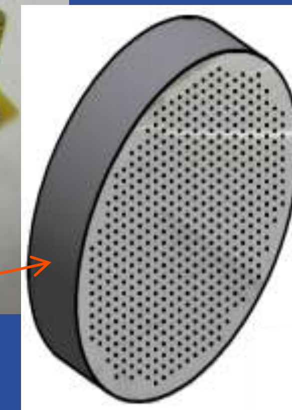


Results and more in paper 8859-32. (Extra...)

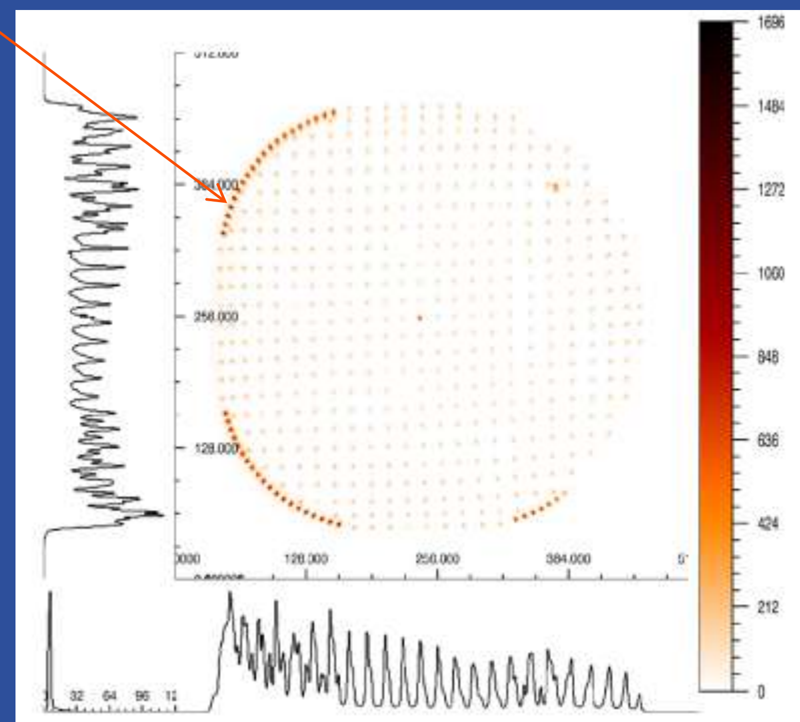
University of Leicester

EXTRA..Prototype



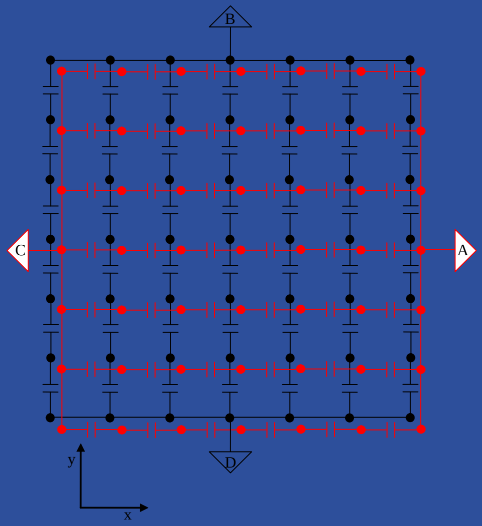


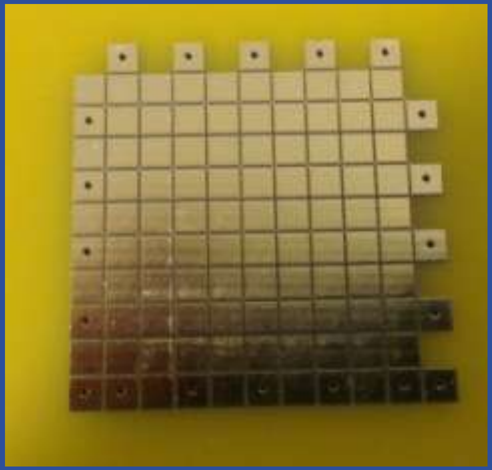
- Prototype C-DIR device; PCB, double-sided array of conductive square pads, 2.54 mm pitch.
- Perimeter capacitance achieved with surface mount capacitors.
- Pinhole array mask image (25 µm & central 50 µm diameter pinholes).
- Proved concept, measured performance limited:
  - Signal loss to the rear MCP contact by parasitic capacitance.
  - Coaxial cable to the CSP =>dominant capacitive load.
  - Optical broadening of image on detector PC (source collimation and diffraction).



Spatial resolution 150 µm FWHM @ ~10^6 electrons.

Extra....C-DIR alternate design





- Alternate design; x and y axes are encoded separately.
- All mutual capacitances define perfect linear dividers; no need for large perimeter capacitances.
- Each axis only benefits from half signal which impacts signal to noise ratio.

Extra....Experimental optical setup