weeroc

High-end Microelectronics Design

ROC chip family

NDIP 2014, Tours

July 4th 2014

Julien Fleury

On behalf of :

- Omega Microelectronics lab
- Weeroc SAS

WEEROC & OMEGA PRESENTATION

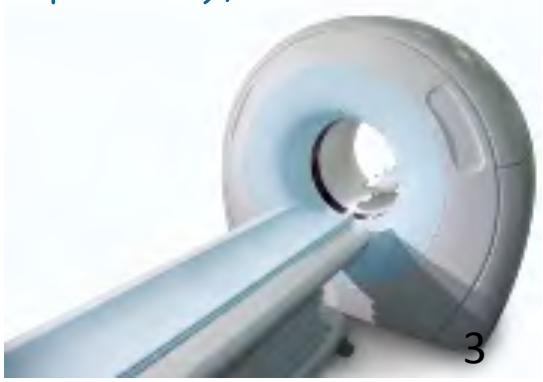
Team, offer, organization

About Weeroc

- Weeroc is a start-up company of Omega laboratory

- Weeroc is located in Orsay (Paris Suburb), France

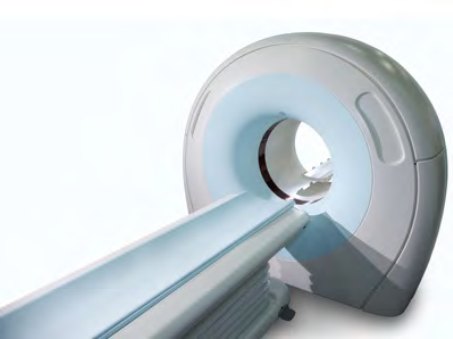
- Weeroc provides :
  - off-the-shelf front-end ASIC (the ROC chip family)
  - customer-specific ASICs
  - Services, Audit, Expertise



Omega microelectronics lab

Research,
Institute

Education,
School



Industry, company

Weeroc offer : application fields

Scientific instrumentation

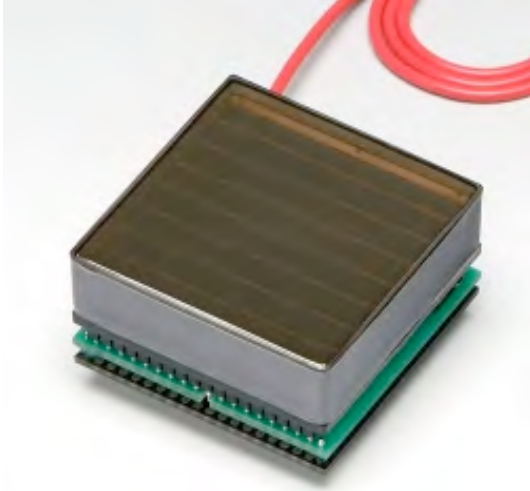
Nuclear industry

Medical imaging

Homeland security

Aerospace industry

Analytical instrumentation

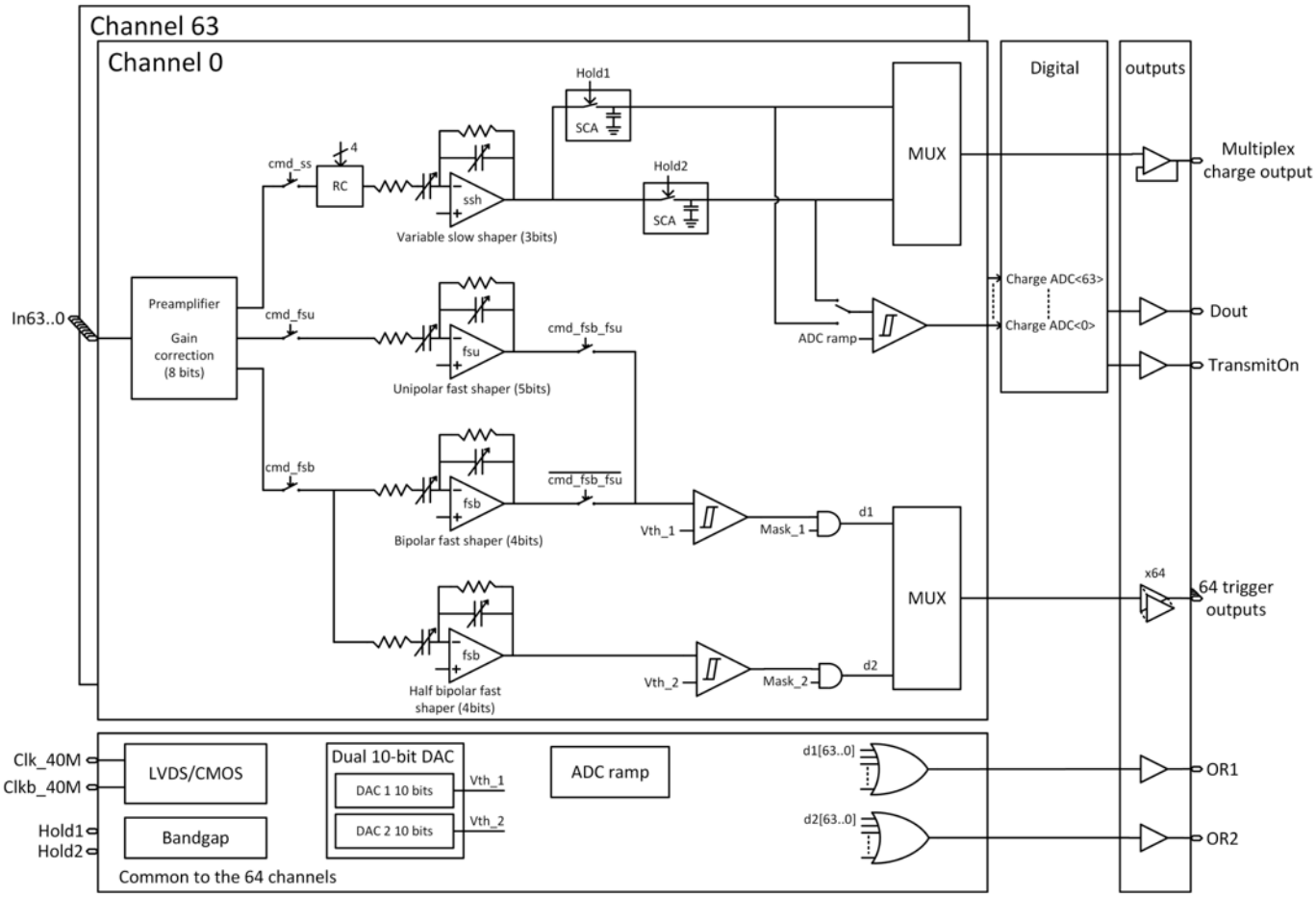


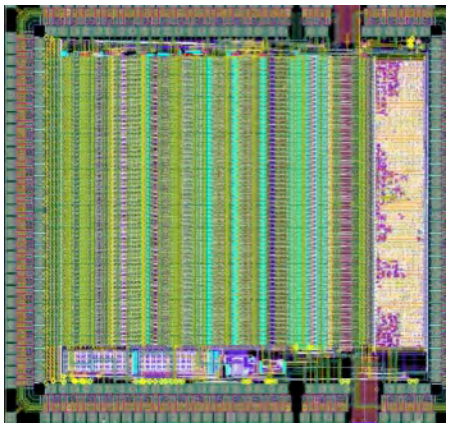
READ-OUT CIRCUITS FOR MULTI-ANODE PMT& PMT ARRAYS

Maroc, Spaciroc, Parisroc

Maroc 3

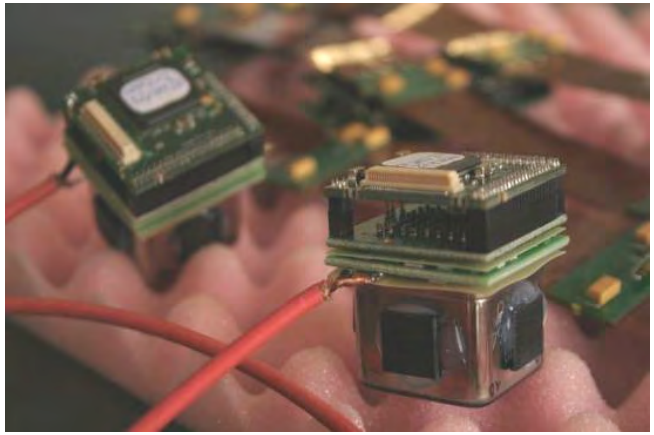
- Complete front-end chip for 64 channels multi-anode photomultipliers
- 6-bit individual gain correction
- 64 trigger outputs, trigger on 1/3 of photo-electron
- Multiplexed charge output and internal ADC (12 bits)



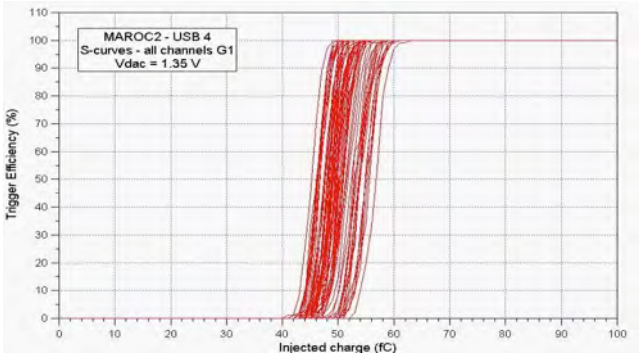


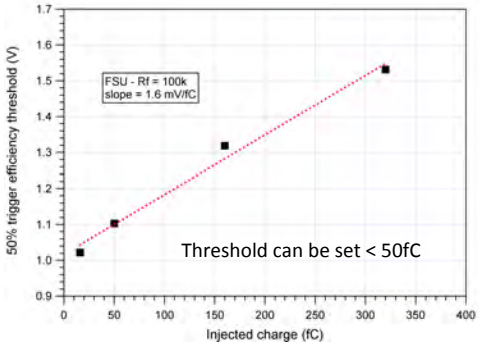
PMF – Atlas luminometry

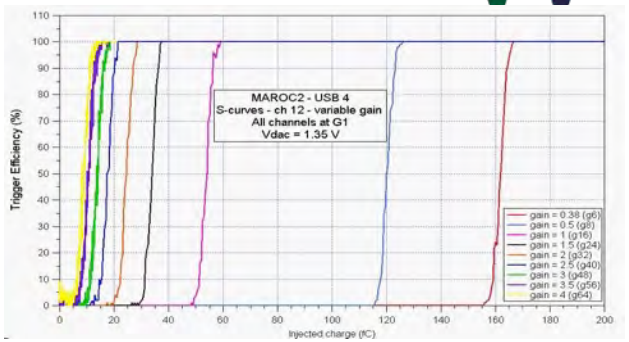
- Get the front-end electronics and HV circuitry in the shadow of the MA-PMT

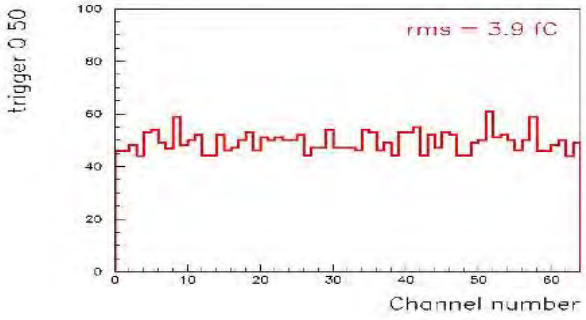


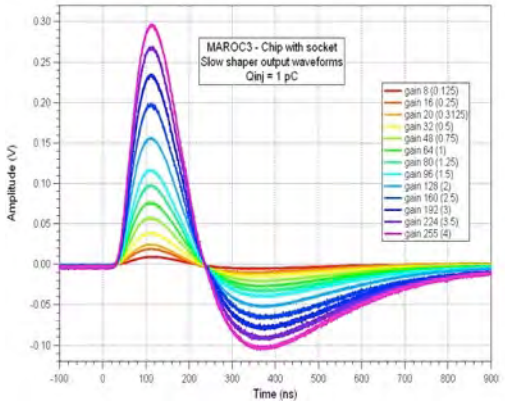
MAROC measurements

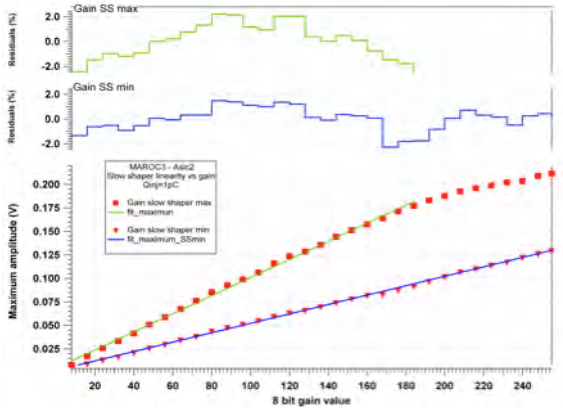


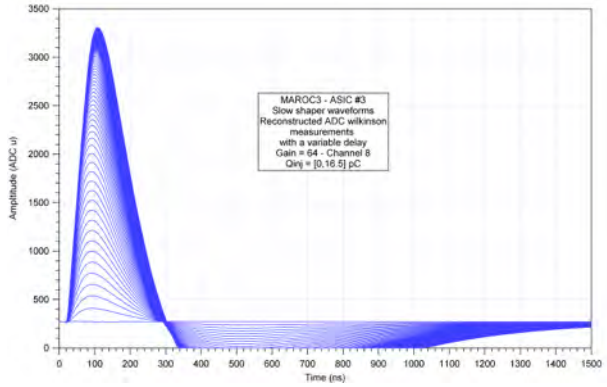


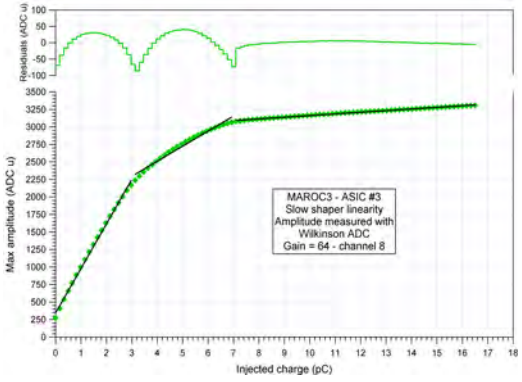






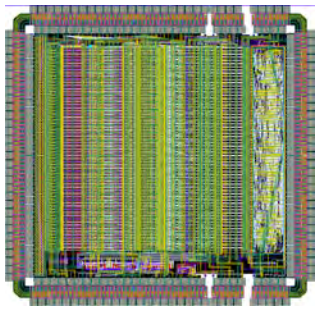


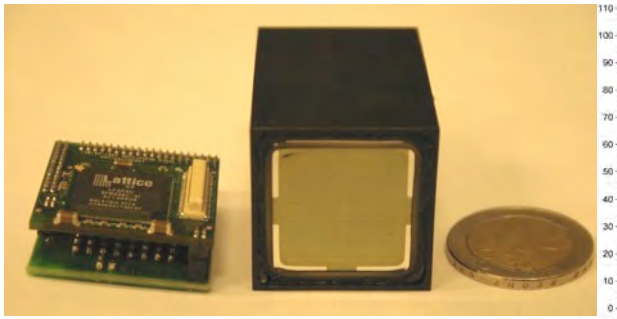


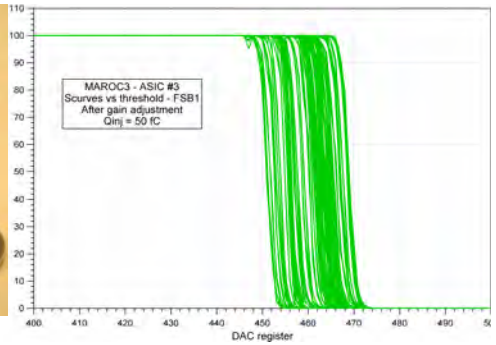


Gain	4	8	16	32	40	64
Slope (adc count/pC)	35	70	148	305	383	636
Intercept (adc count)	271	271	269	265	262	271
Fit limit (pC)	30	20	10	5	4	3

MAROC3 users







2012-2013	
Ralf ENGELS	Allemagne/Juelich
Vladimir SOLOVOV	Portugal/ Coimbra
Scott Lumsden	UK/Glasgow
JJ Velthuis	UK/Bristol
Piero Giorgio FALLICA/ ST micro	Italie/ Catania
Vincent TATISCHEFF	France/Orsay
Alexander Nadeev	Russie
Domenico Lo Pesti	Italy/Catania
E.L. Rizzini	Suisse/Genève
D. Lo Presti	Italie/ Catania
P. Rodrigues	Portugal/Lisboa
Stephen Wotton	Suisse/Genève
JJ Velthuis	UK/Bristol
Riccardo Faccini	Italie/Roma
Patrizia Rossi	Italie/Frascati
Sima Cristina	Roumanie/Magurele
Patrizia Rossi	Italie/Frascati
D.Cussans/P.Baesso	UK/Bristol
Paolo Baesso	UK/Bristol

Alain Blondel	Suisse/Genève
Pedro Rodriguez	Portugal / Lisboa
William Brooks	Chili / Valparaiso
Stephane Colonges	France / Paris
Evandro Lodi Rizzini	Suisse / Genève
Günter Kemmerling	Allemagne/Juelich
Thomas Schweizer	Allemagne/Munich
Jason Legere	USA / Durham
Evandro Lodi Rizzini	Suisse / Genève
Ronan Oger	France / Paris
Erik Vallazza	Suisse / Genève
Daniel Bertrand	Belgique / Bruxelles
Ronan Oger	France / Paris
Jason Legere	USA / Durham
Tanushyam Bhattcharjee	Kolkota/Inde
Vincent Tatischef	France / Orsay

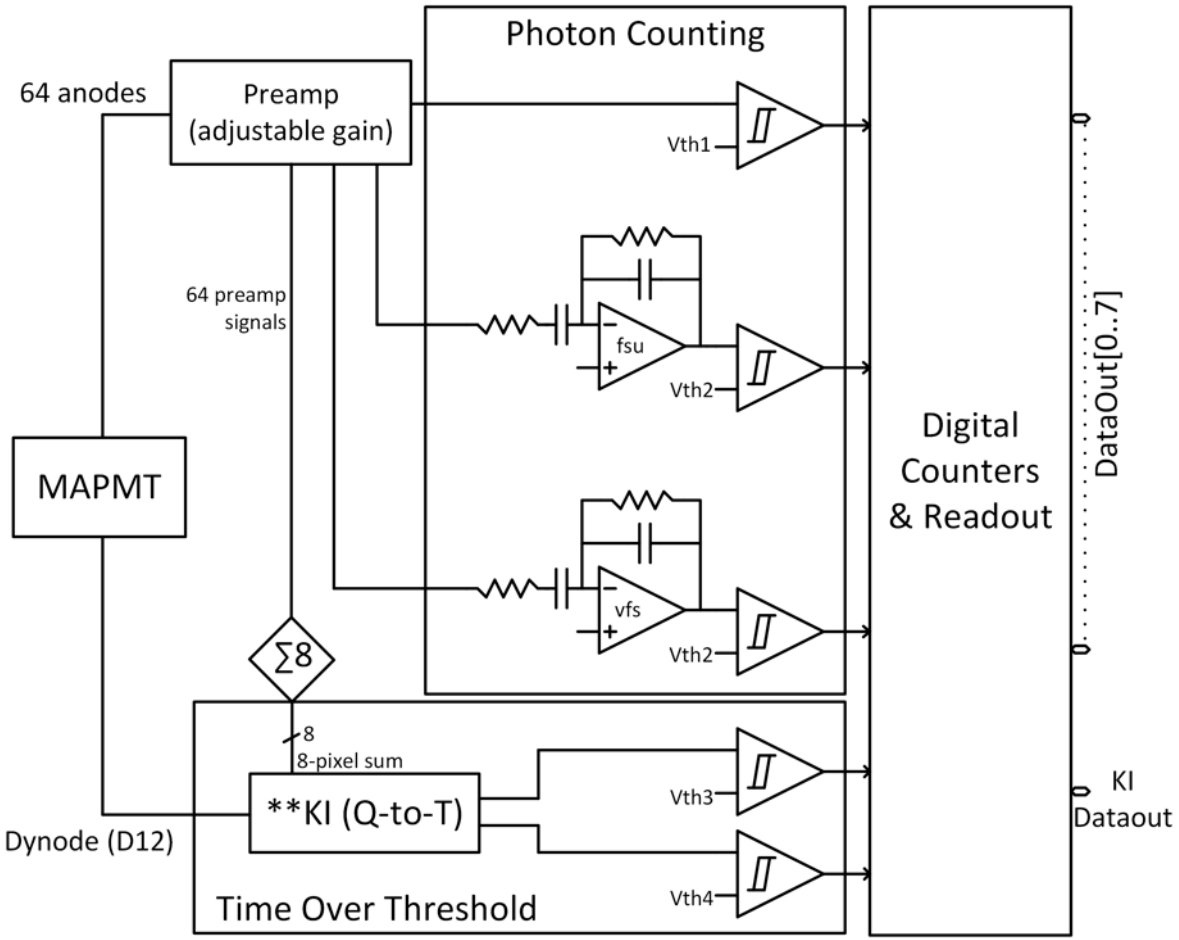
Gabriela Llosa	Espagne / Valence
Pierre Salin	Sofia Antipolis/France
Prof. A.A.Petrukhin	Russie/Moscou
Erik Vallazza	Suisse / Genève
Riccardo Faccini	Roma/Italie
Pierre Salin	Sofia Antipolis/France
Prof. A.A.Petrukhin	Russie/Moscou
Bernard Genolini	France / Orsay
Nicoleta Dinu	France / Orsay
JJ Jaeger	France / Paris
Vincent Tatischef	France / Orsay

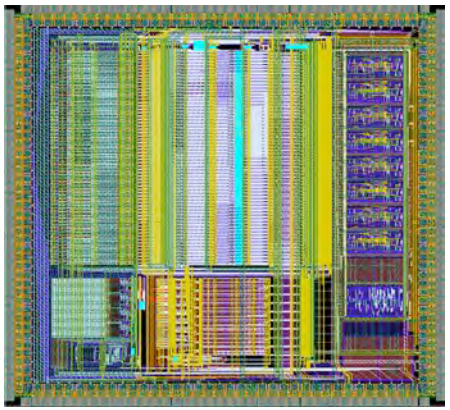
- ATLAS lumi : 500chips (LAL)
- Double Chooz : 1000 (Nevis)

- CLAS12 RICH (INFN)
- LHCb RICH ? (CERN)
- JUNO ? (IPHC)

Spaciroc 3

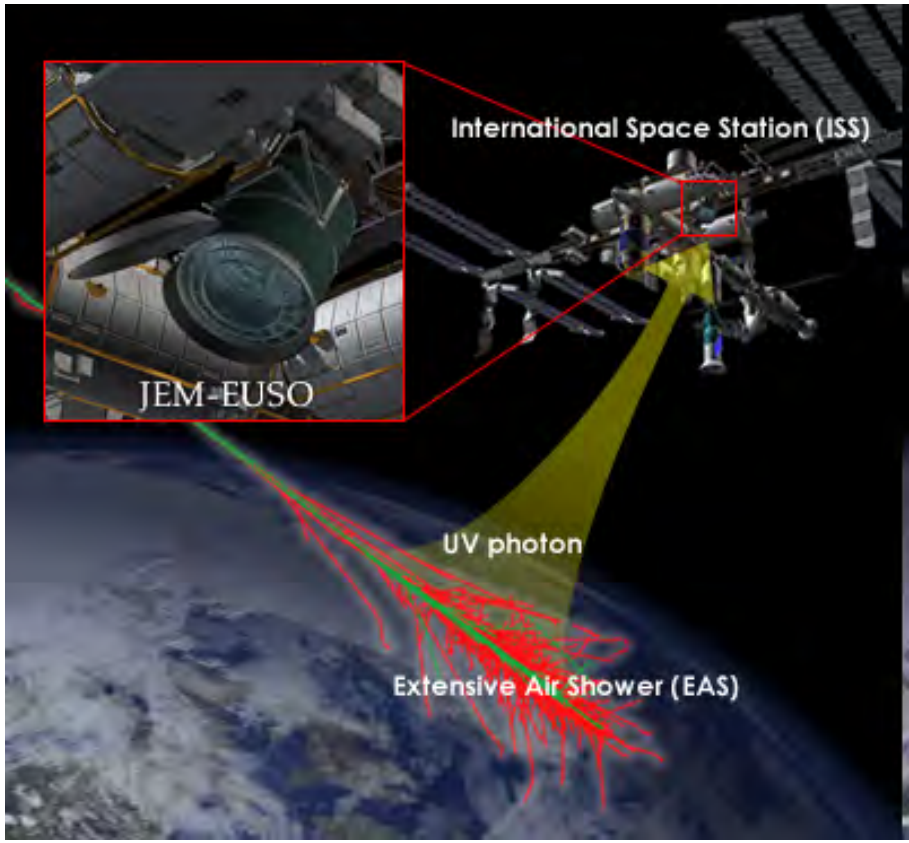
- MAROC variant : Complete front-end chip for 64 channels multi-anode photomultipliers
- Photon counting : 50MHz
- Time-over-Threshold for energy measurement





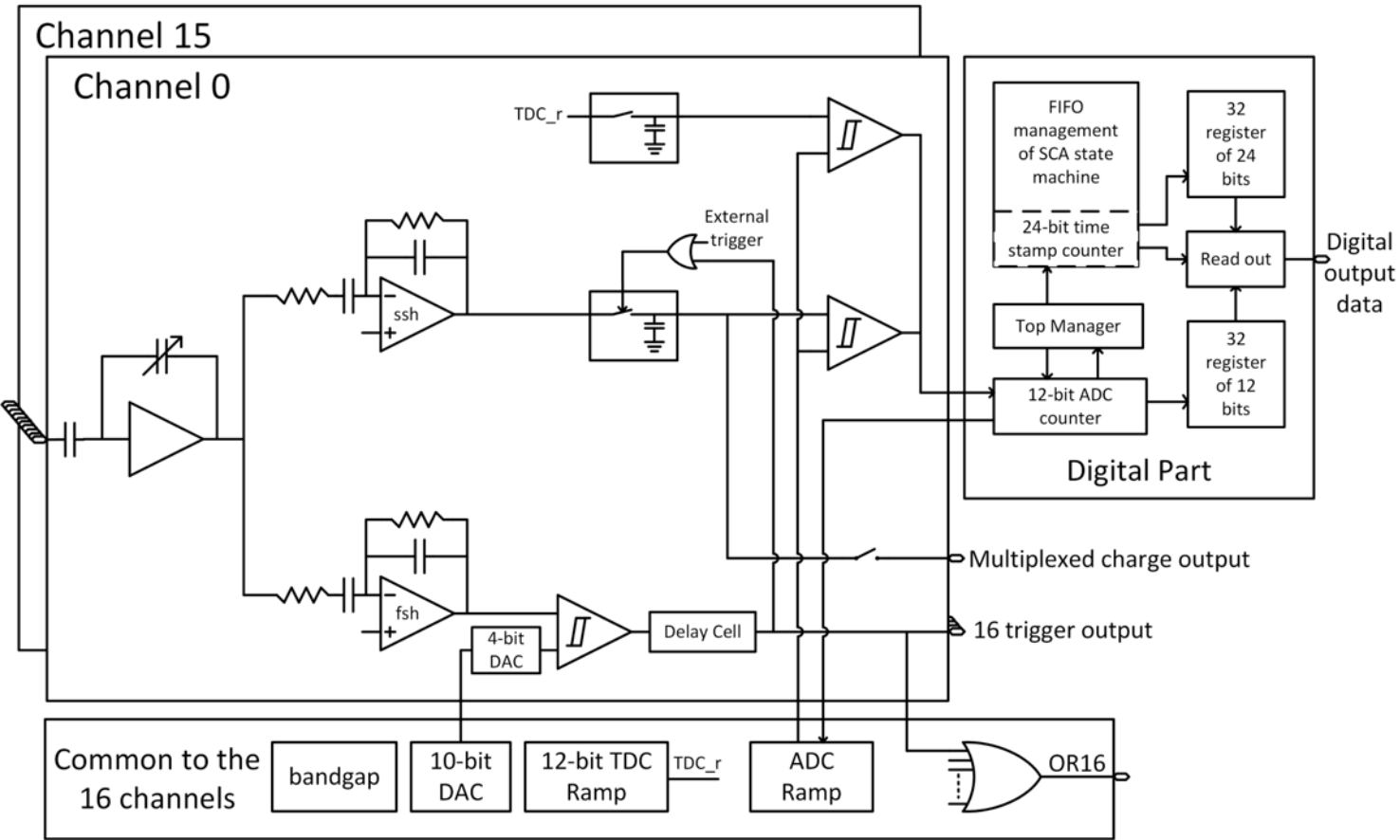
JEM-EUSO

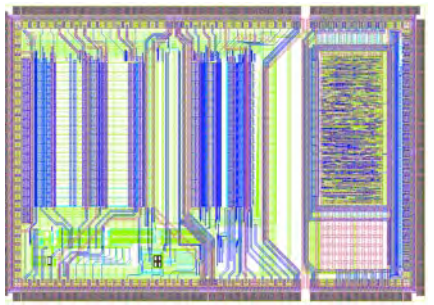
- Power consumption < 1 mW/ch
- Radiation tolerance : triple voting



Parisroc 2

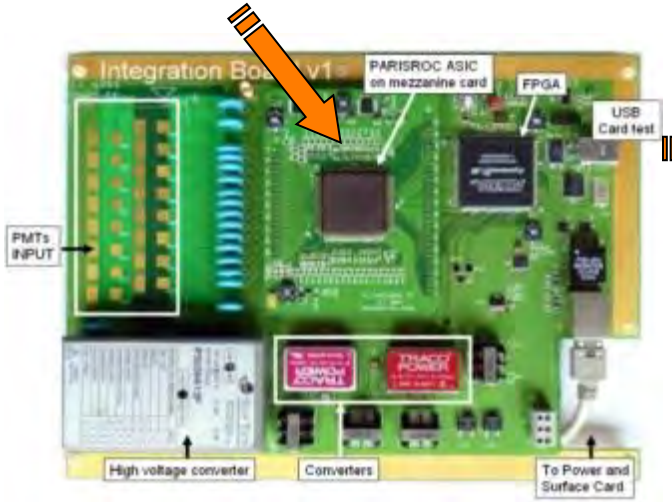
- Replace large PMTs by arrays of smaller ones (PMm2 project)
- Centralized system-on-chip ASIC : 16 independent channels
- Auto-trigger at 1/3 p.e.
- Charge and time measurement (10-12 bits)
- Water tight, common high voltage
- Data driven : « One wire out »





PMm2 demonstrator

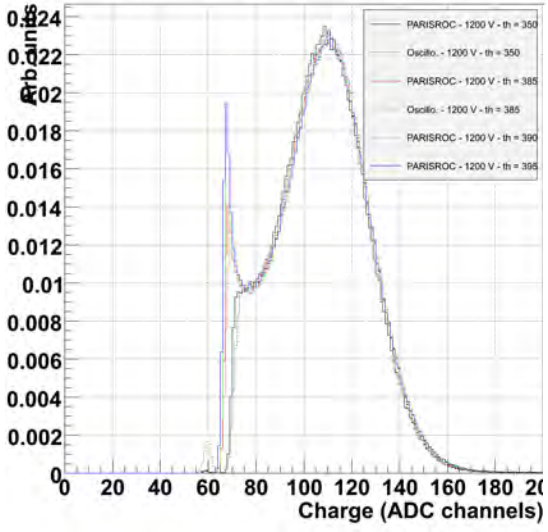
PARISROC2 chip



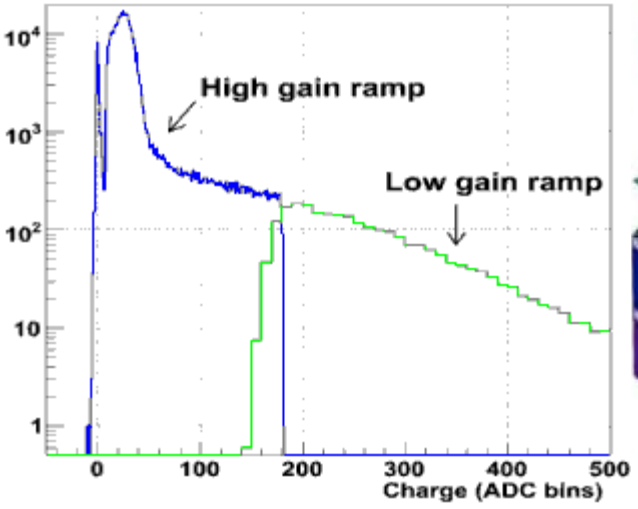
Watertight box

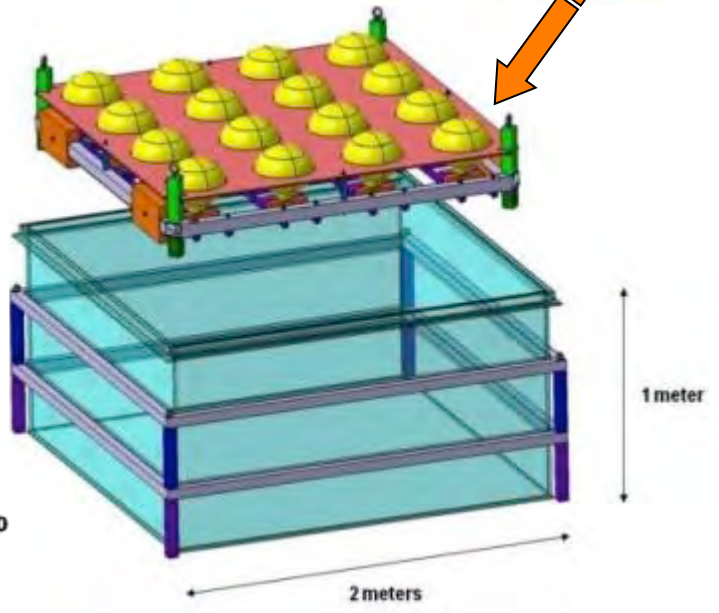
2m x 2m array

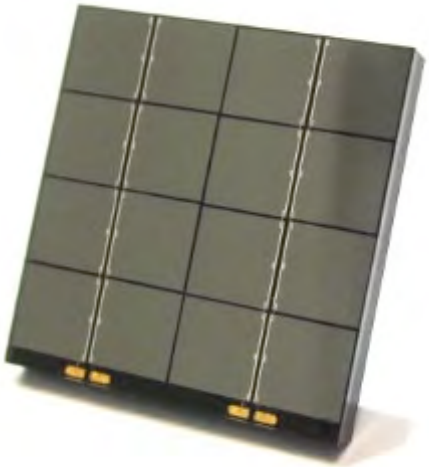
1-in (XP3102) single p.e. noise spectrum.

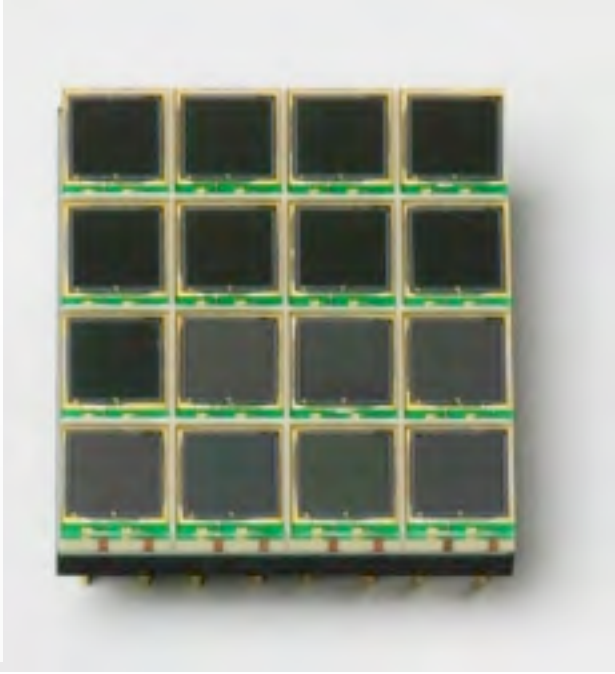


8-in (Hamamatsu R5912)
Single p.e. noise spectrum.







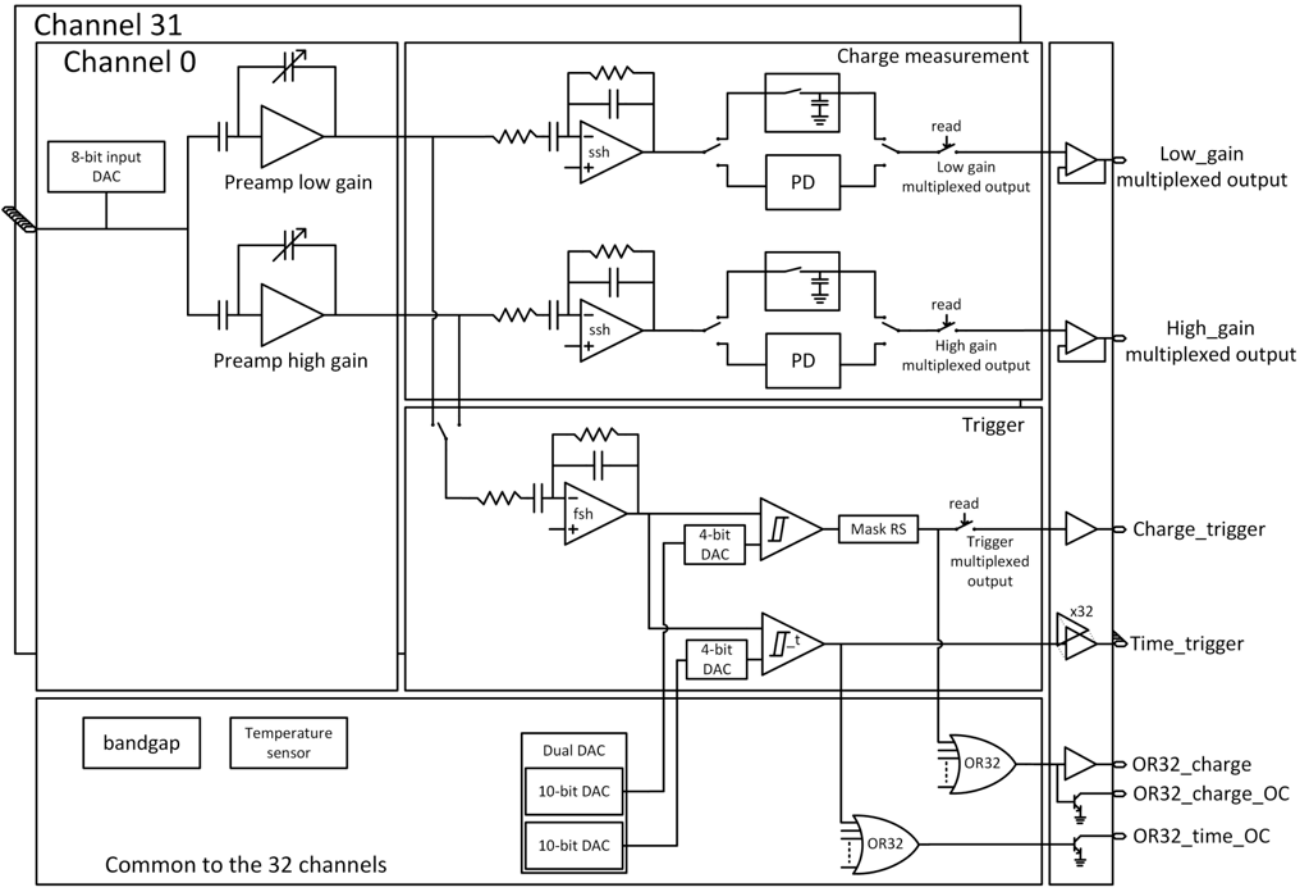


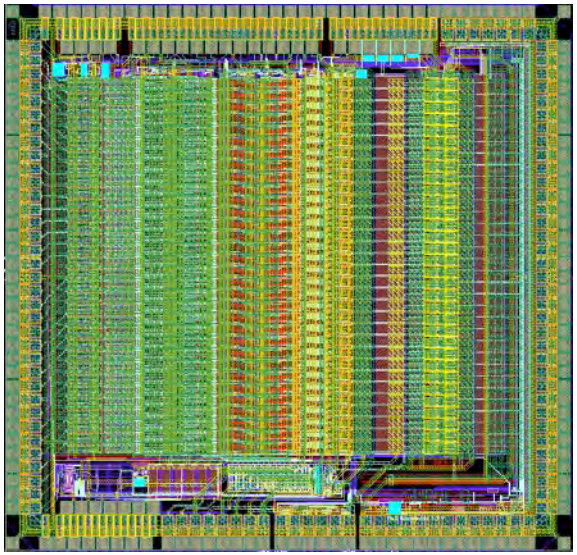
READ-OUT CIRCUITS FOR SIPM

Citiroc, Petiroc, Triroc

Citiroc

- Evolution of Easiroc ASIC : analogue front-end chip
- 32 channel, positive input, input dac HV adjustment
- 32 trigger output & multiplexed charge output
- Peak detector & two trigger level (timing & energy)

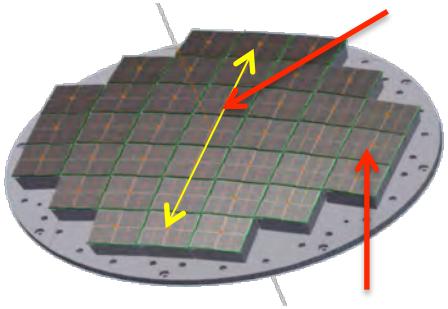




CTA : small telescopes

FOV = 9.6°

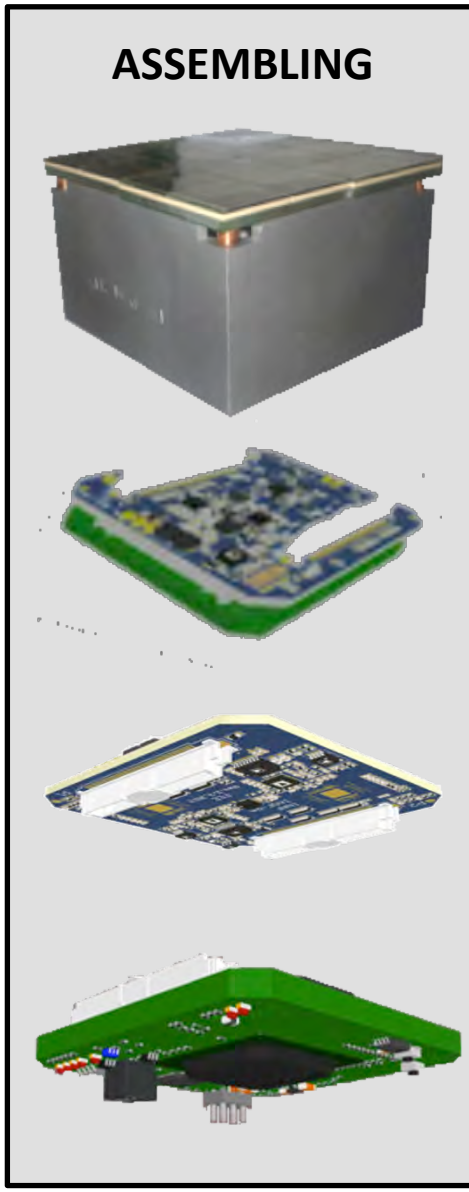
Ø = 350mm

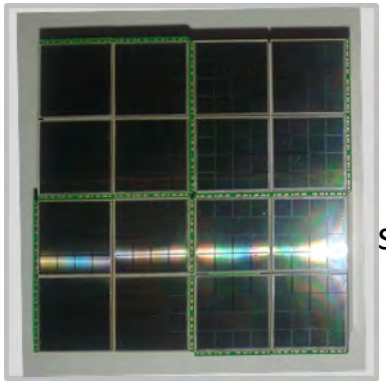


Photon Detection Module (PDM)

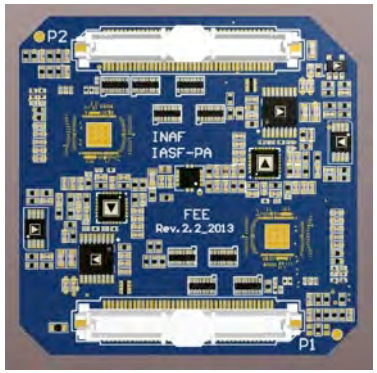
Pixel = 0.17° → 6.2 x 6.2 mm

ASSEMBLING





SiPM board
(9 +1 temperature sensors embedded

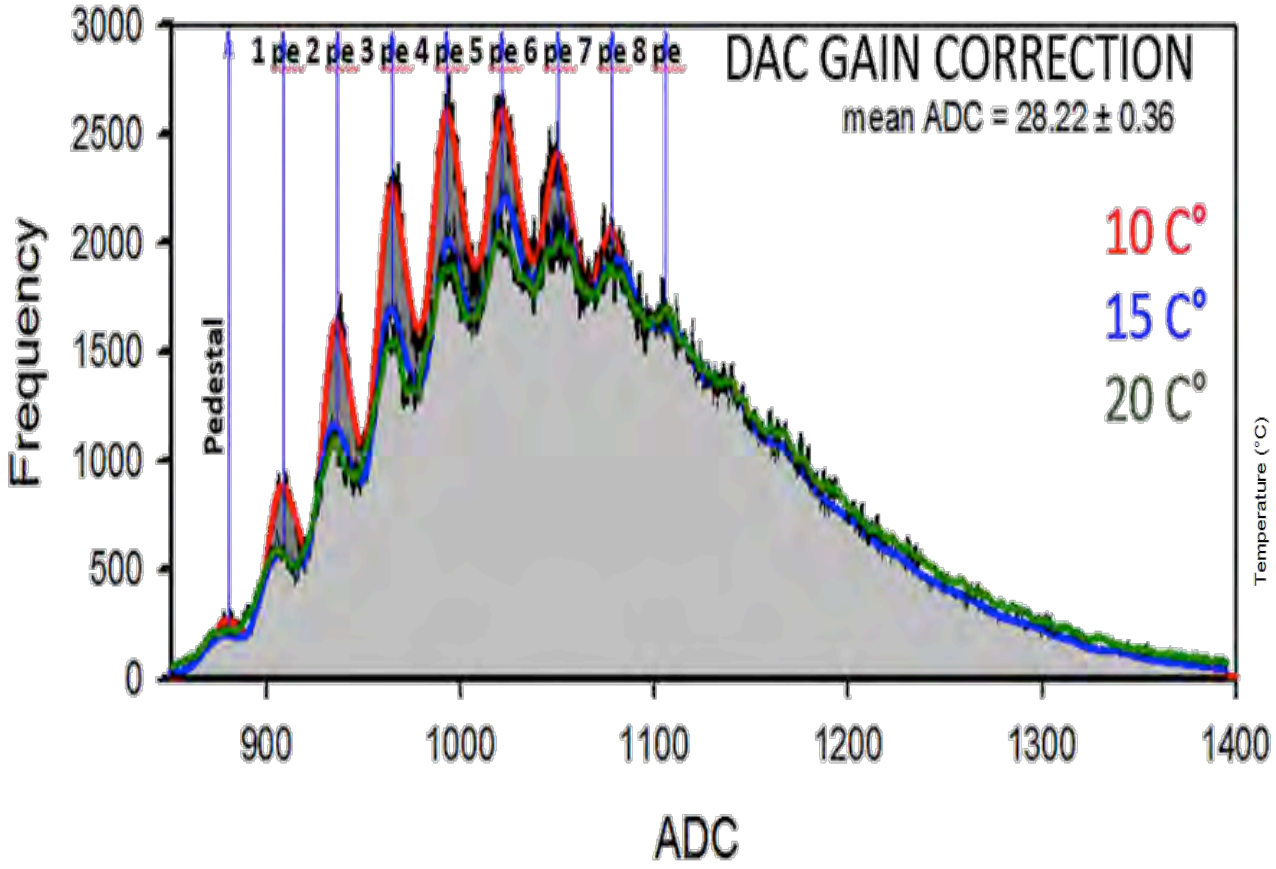


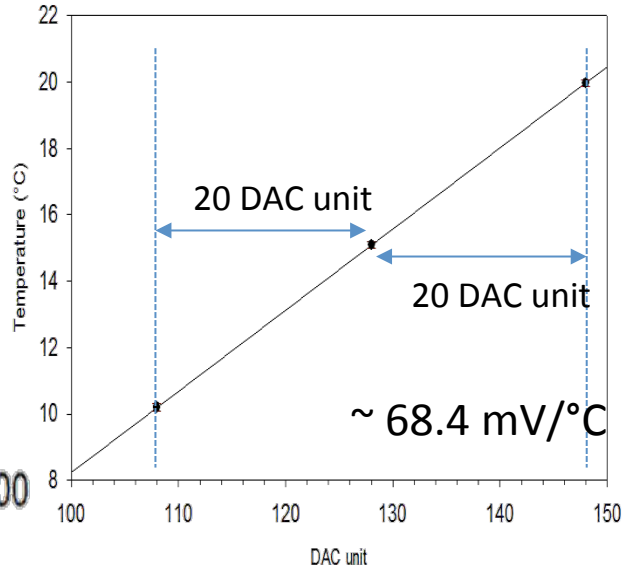
Front-End board
(2 CITIROC ASIC)

PDM FPGA Board
(XILINX ARTIX 7)

Osvaldo Catalano & Al

Practical use of input DAC : gain stabilization

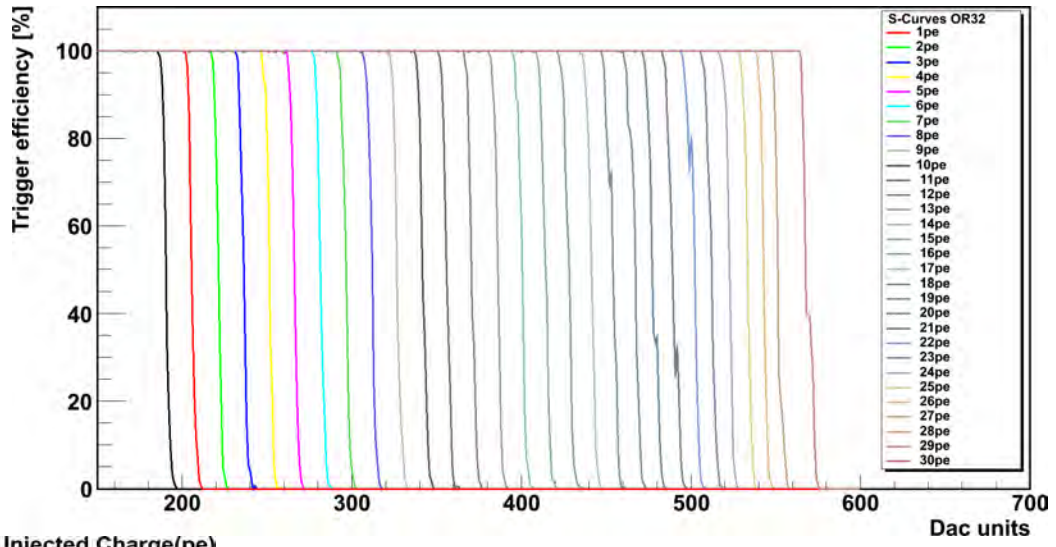


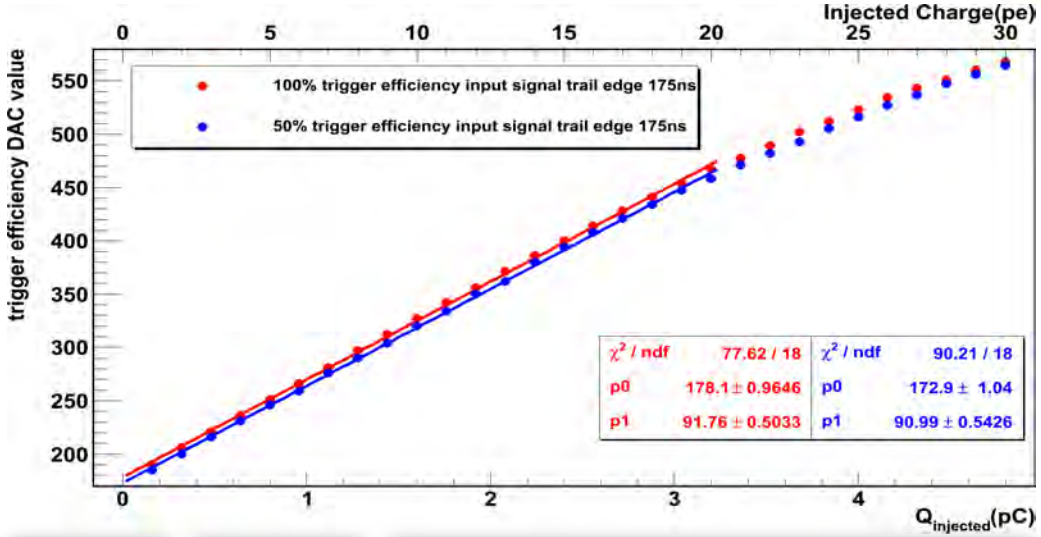


Osvaldo Catalano & Al

Citiroc trigger linearity

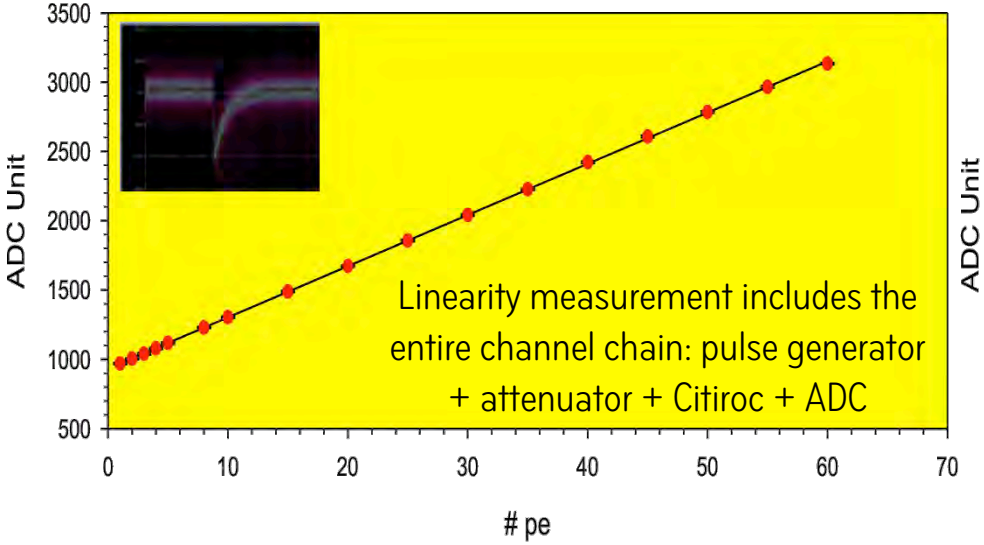
- Trigger linearity < ± 0.3%
- Trigger on 1/3 of a photoelectron
- 10 bits on 2.25V reference => 2.2 mV
- LSB Reference voltage can be adjusted with external resistor.

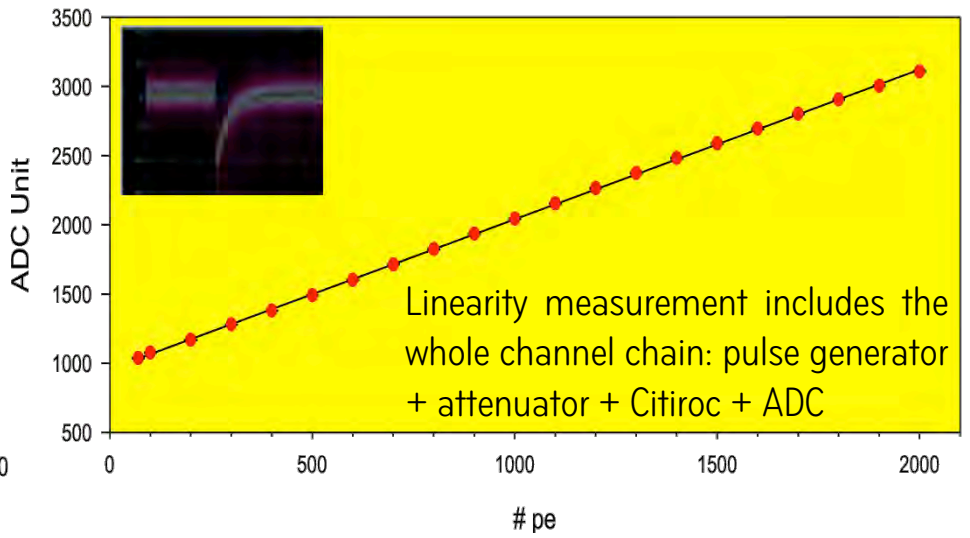


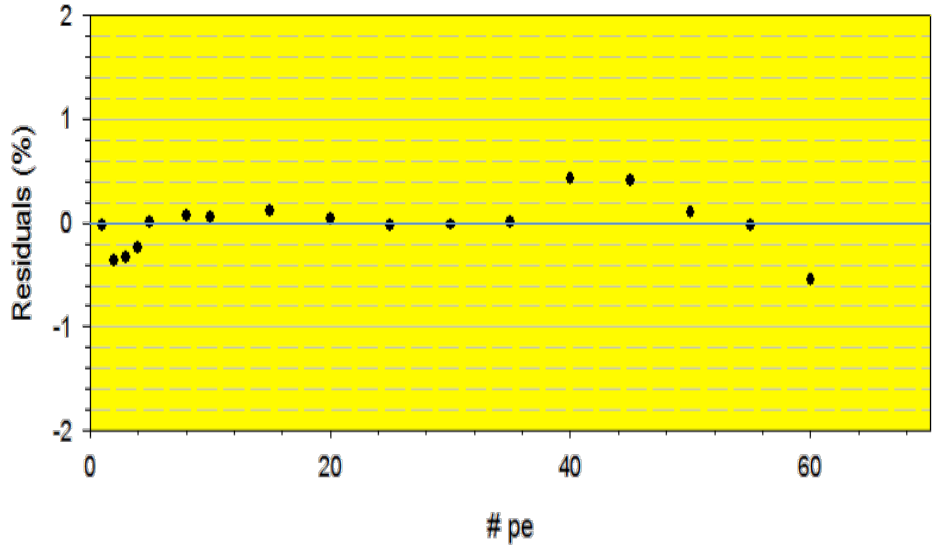


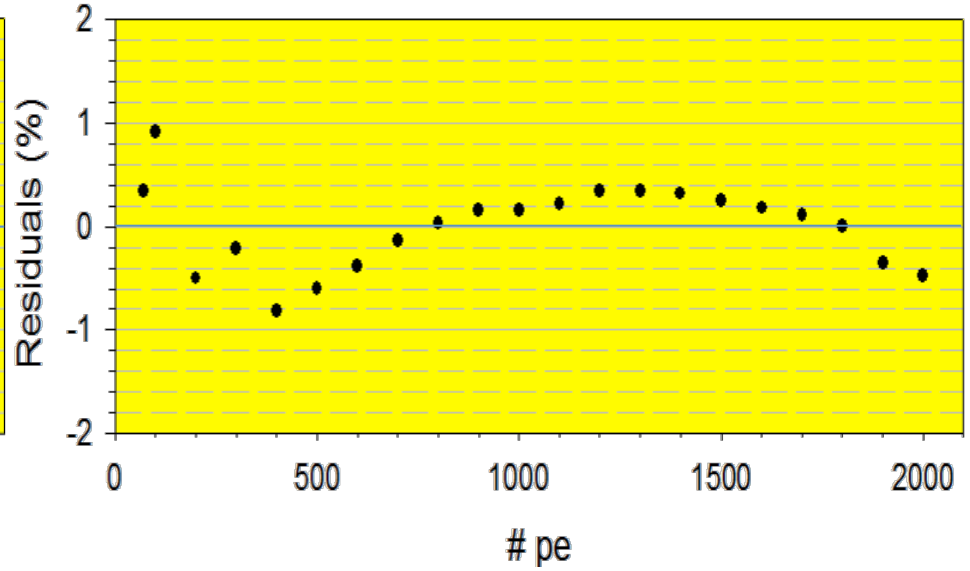
Osvaldo Catalano & Al

Charge measurement : linearities









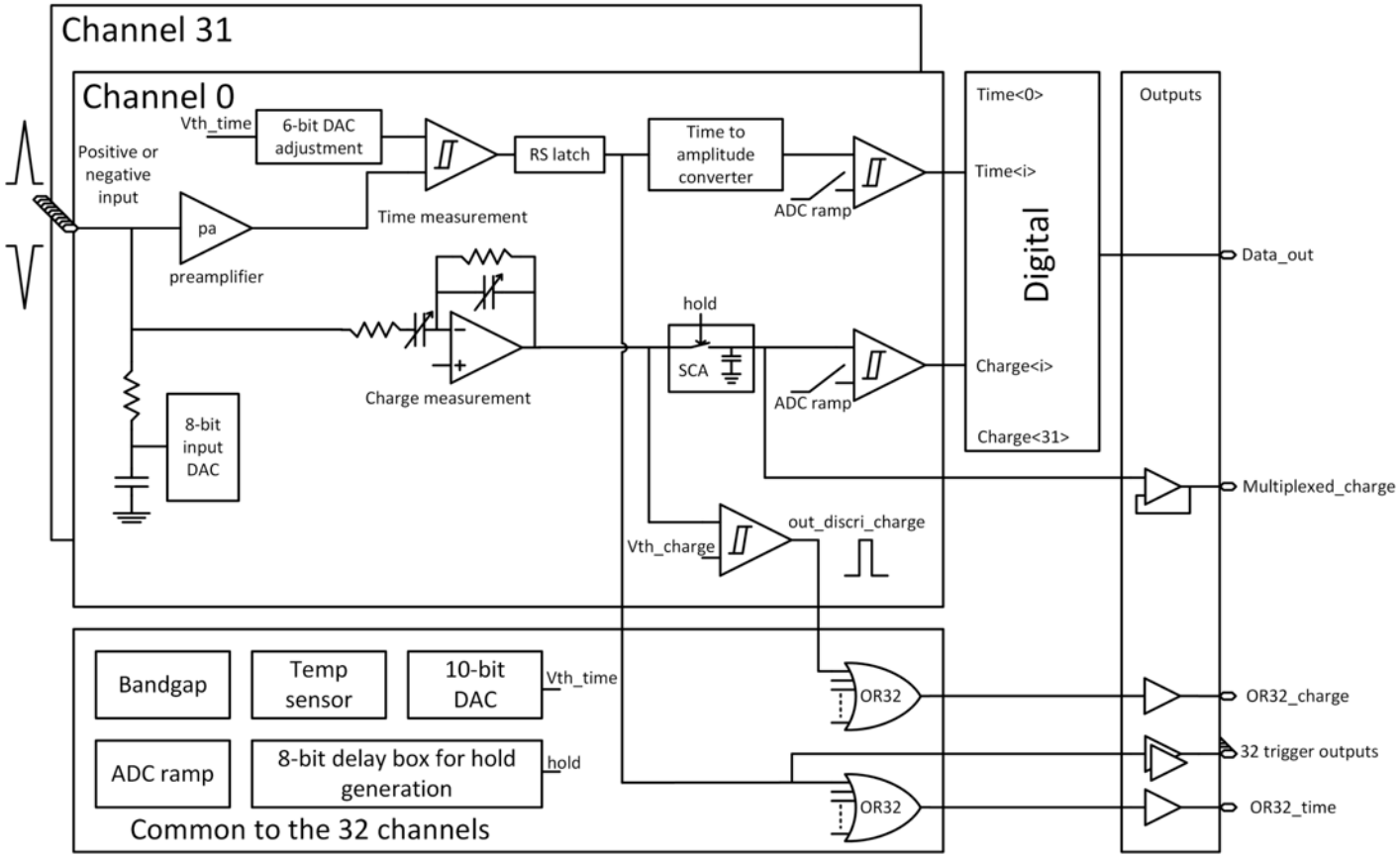
High gain

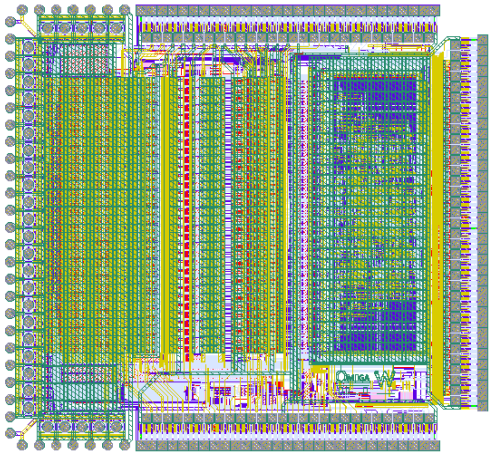
Osvaldo Catalano & Al

Low gain

Petiroc 2

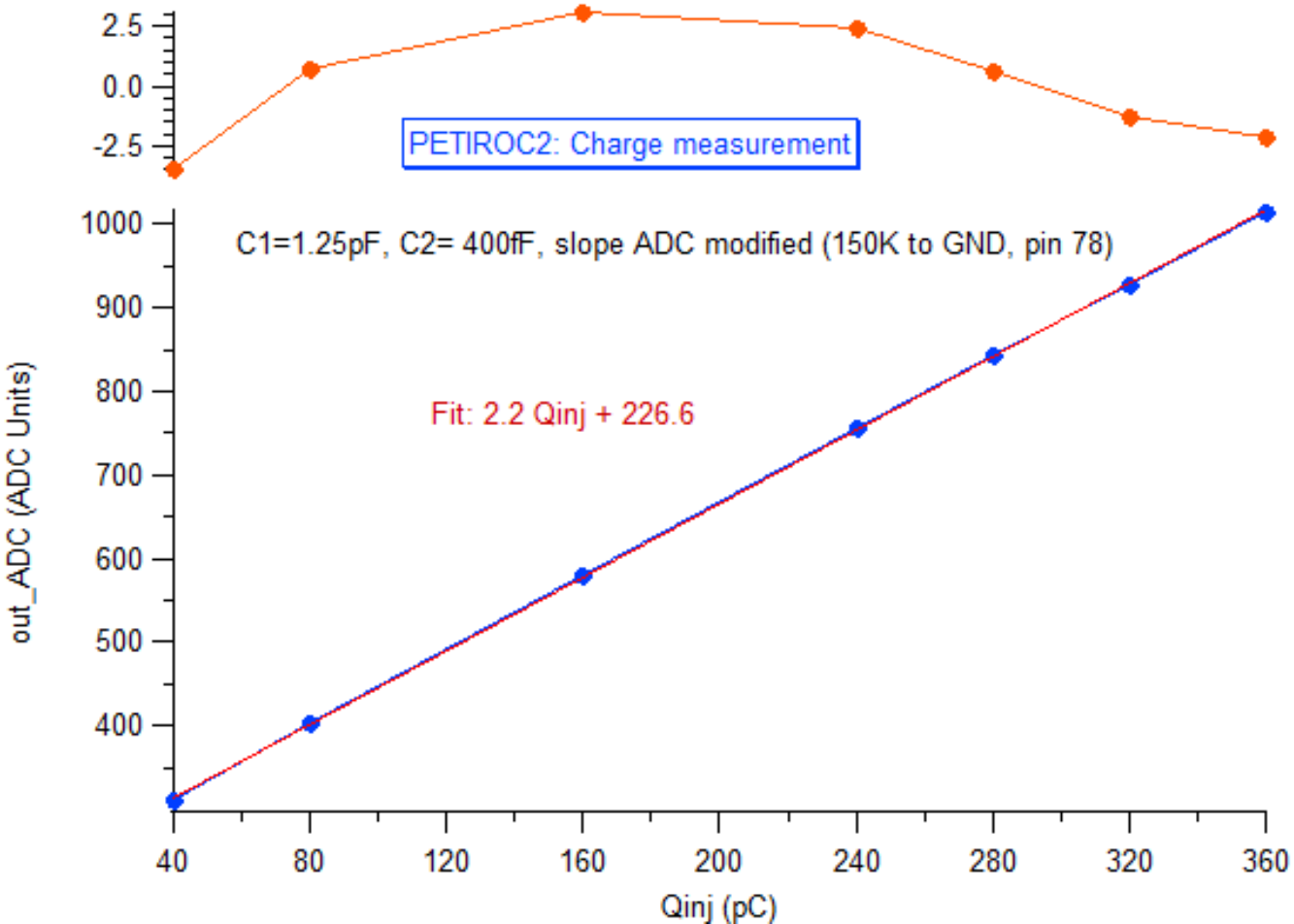
- Time of Flight read-out chip with **embedded TDC** (25 ps bin) and **embedded ADC** (10 bit)
- Dynamic range: 160 fC up to 400 pC
- 32 channels (bipolar input)
- 32 trigger outputs, digital and multiplexed analogue energy output
- Common trigger threshold adjustment and 6bit-dac/channel for individual adjustment
- **Power consumption 6 mW/ch.**
- **Dual trigger level : on first photons and on energy**



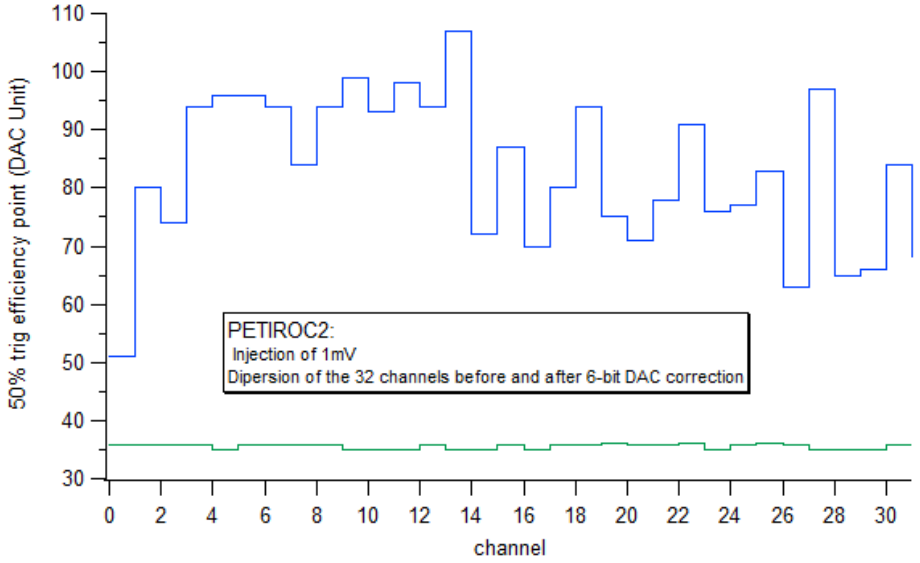


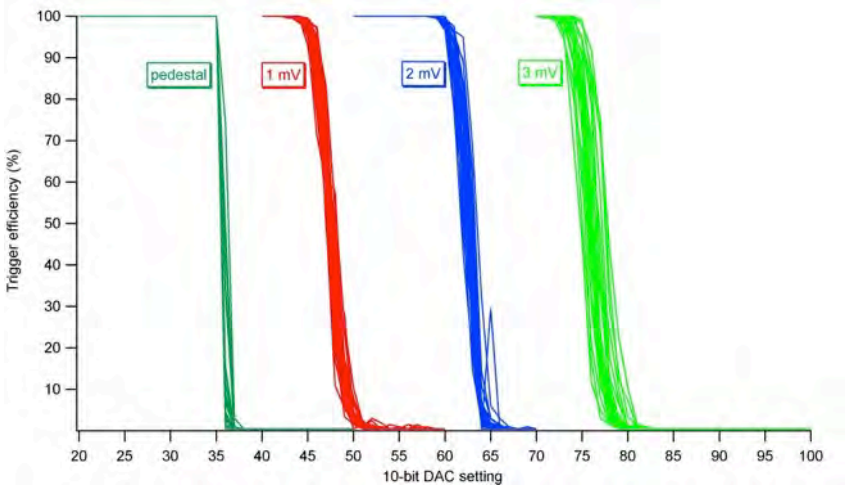
Charge measurement

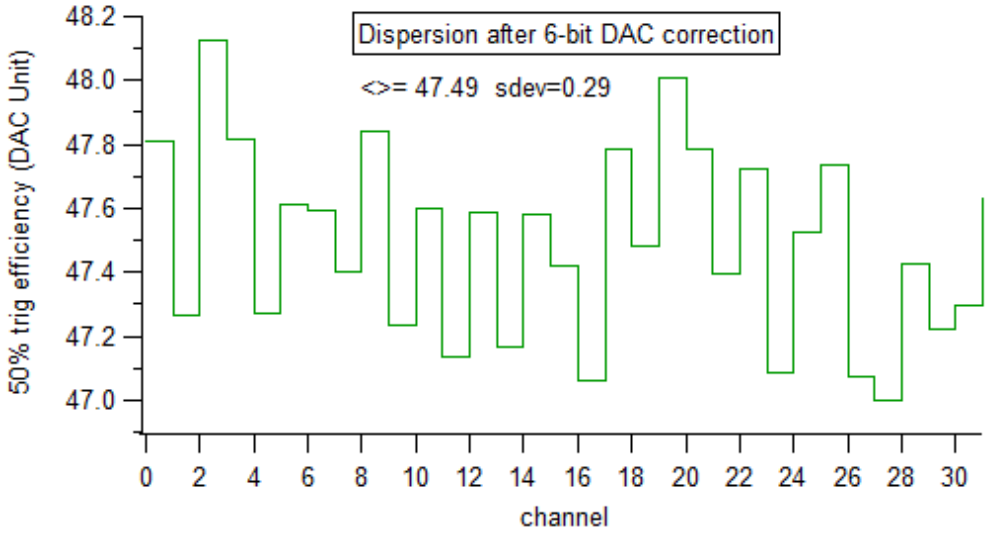
- Energy measurement using Petiroc2 internal ADC
- Measurements made with minimum gain setup to go up to 360 pC

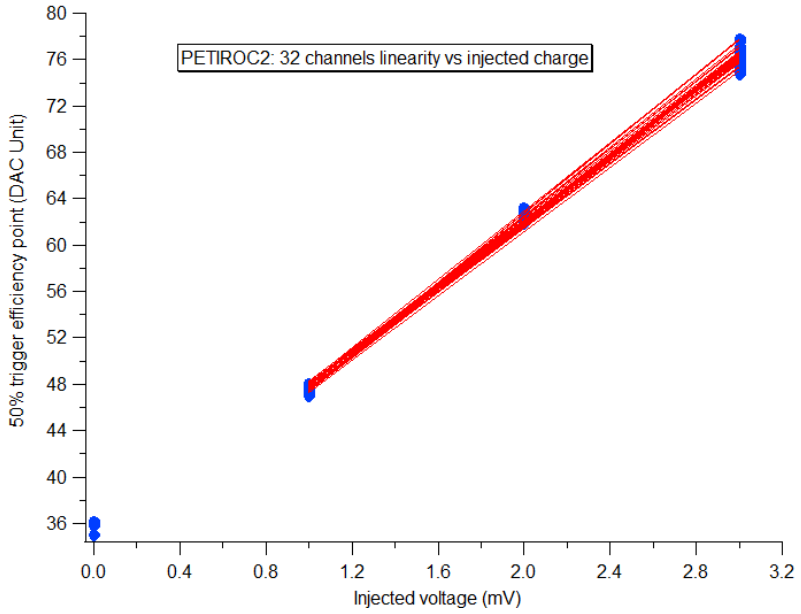


Trigger sensitivity



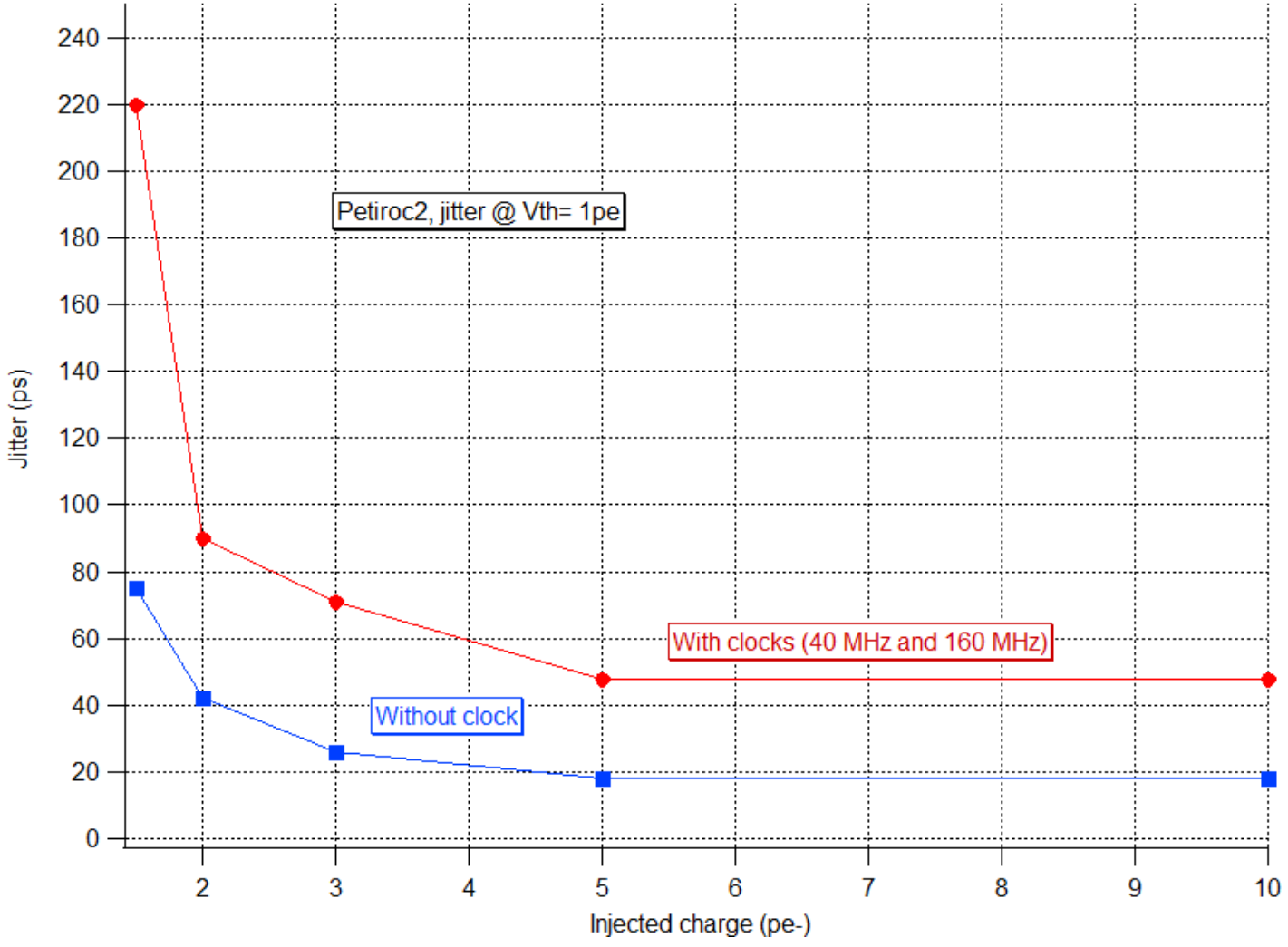




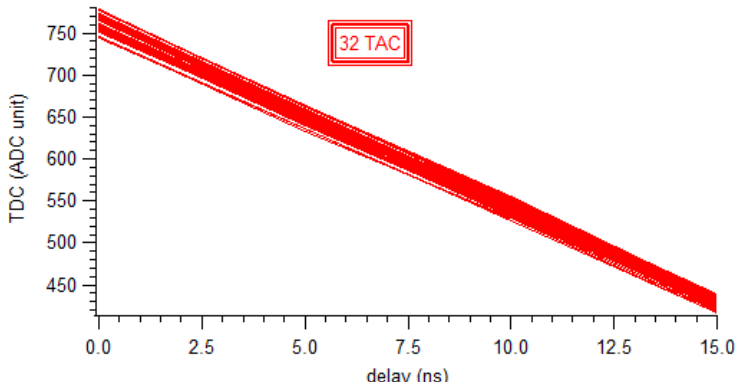


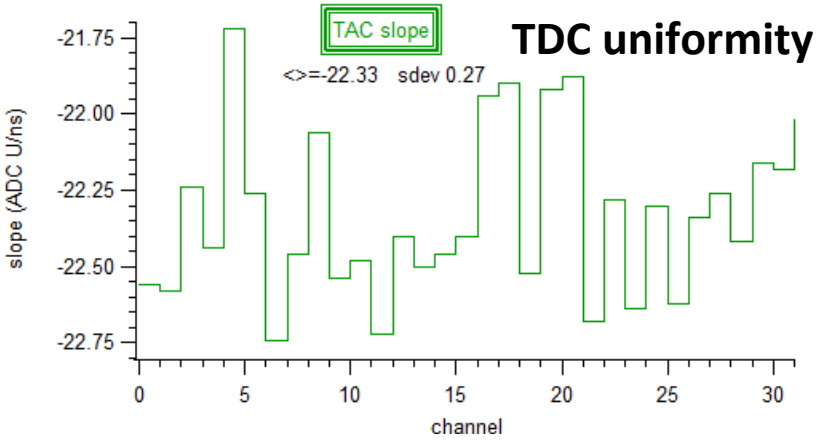
Time resolution with test pulse

- Jitter (ps RMS) versus injection
- With and without internal clock

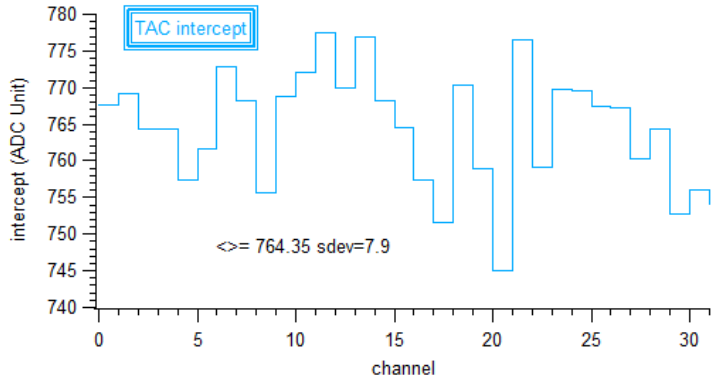


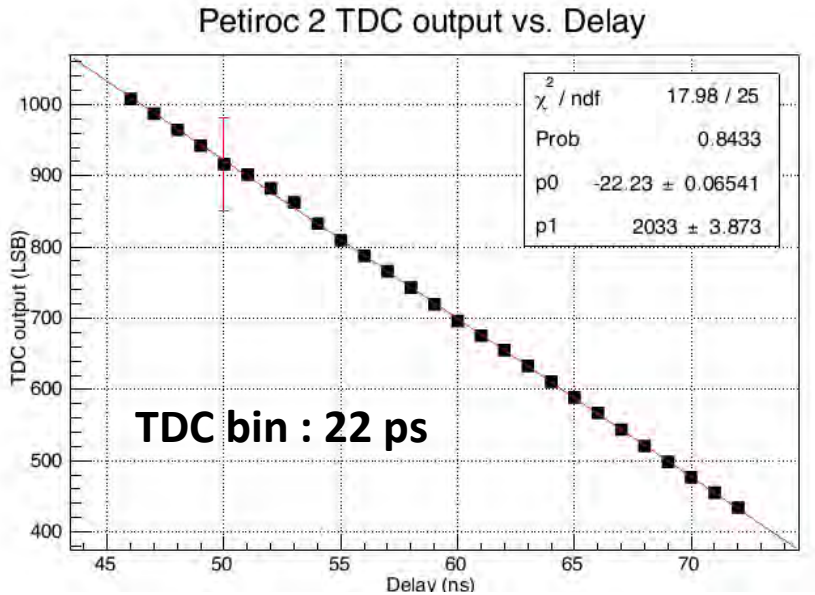
Time resolution : internal TDC



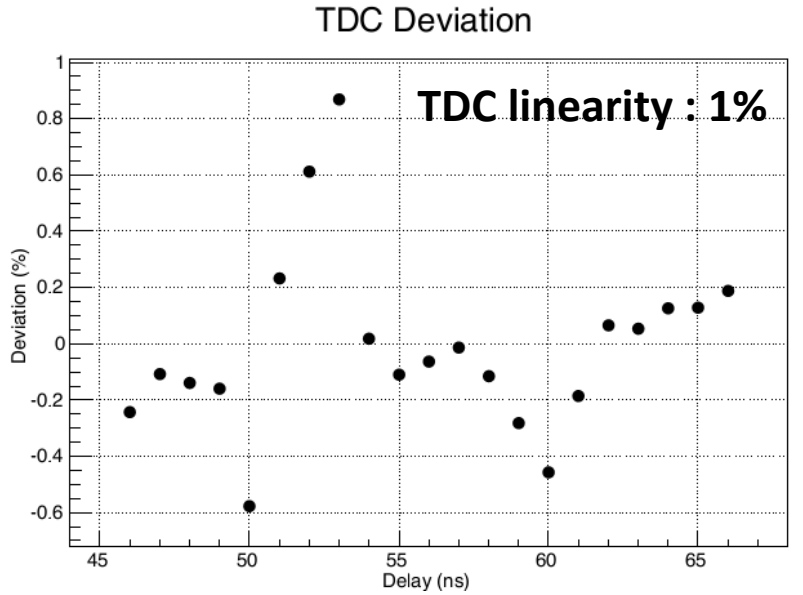


TDC uniformity : 1%





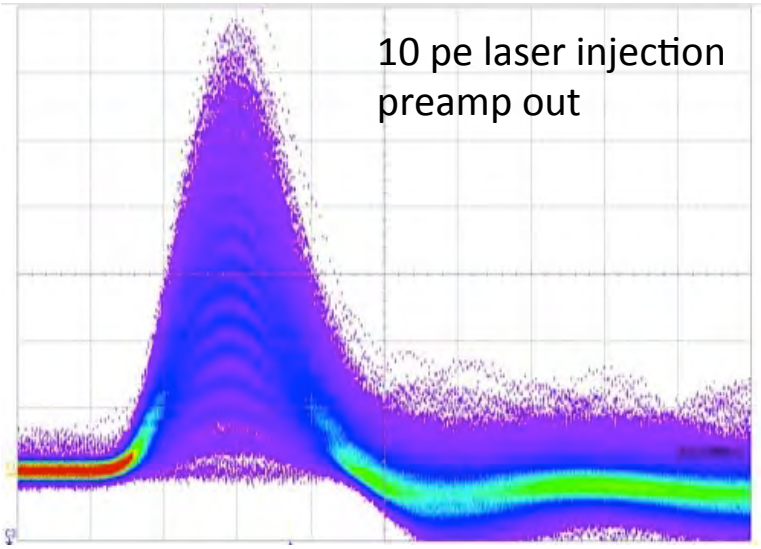
TDC bin : 22 ps



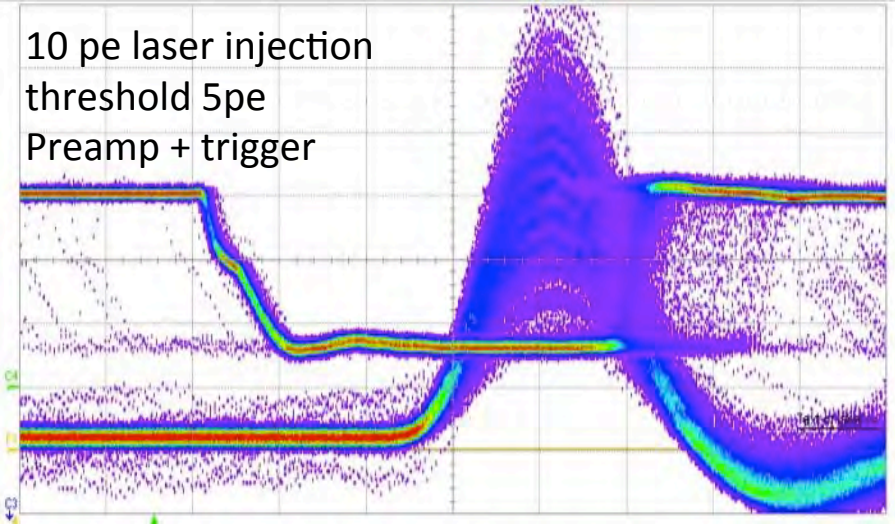
TDC linearity : 1%

Trigger on first photons (Petiroc 1)

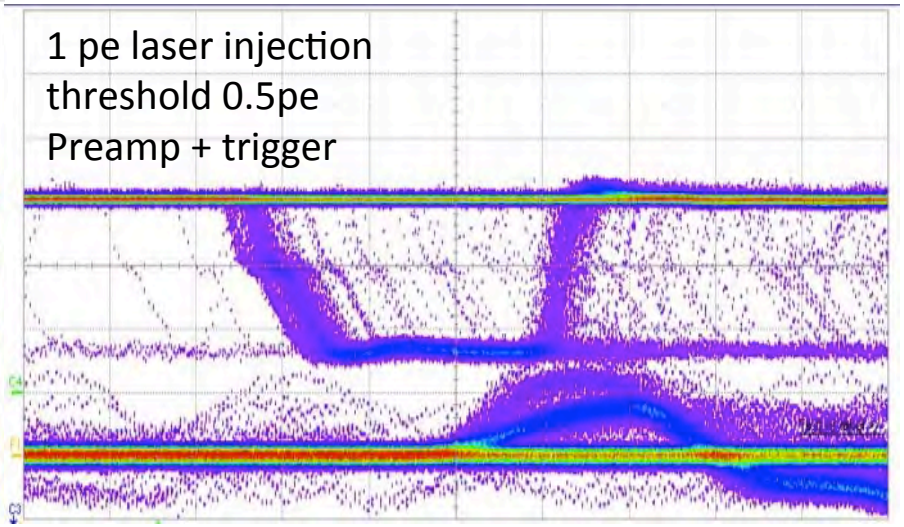
- 1x1mm SiPM Hamamatsu
- Laser for low light injection
  - 405nm
  - Jitter : 28 ps FWMH
- Low trigger mandatory for good timing resolution
- Petiroc can trigger on first photoelectron
- Petiroc is low noise : single photon identification



2 ns/div



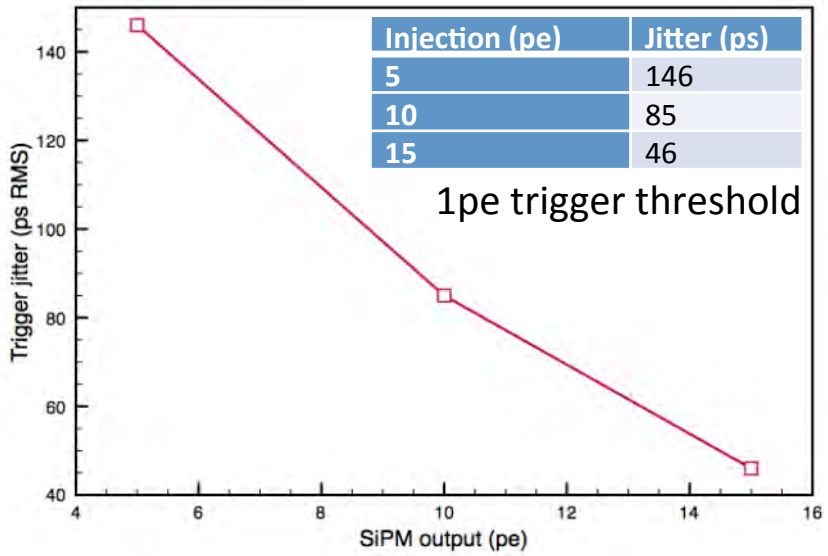
2 ns/div



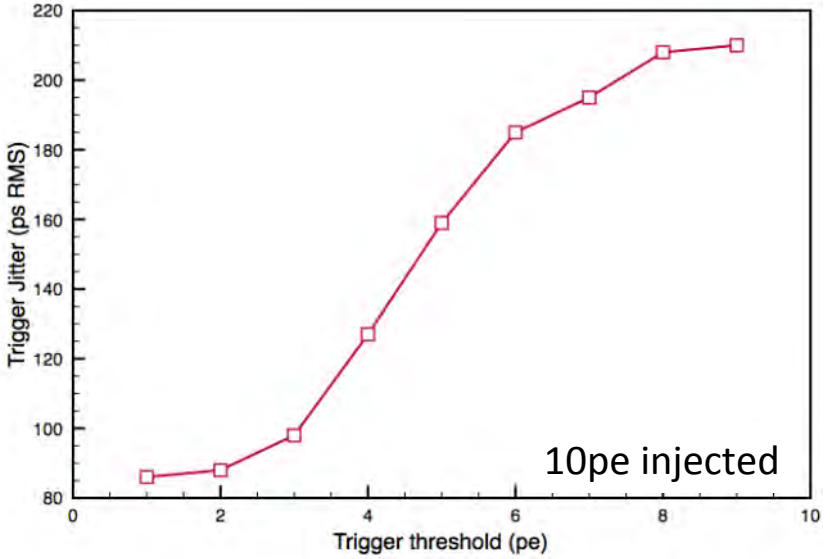
2 ns/div

Time measurement (Petiroc 1)

- Jitter vs injection
  - Laser illumination of SiPM
  - 5 →15 pe, threshold 1pe
  - Jitter improve with signal, down to 50ps
- Jitter vs threshold
  - Laser illumination of SiPM
  - 10pe, threshold 1pe→9pe
  - Jitter improve with lower threshold



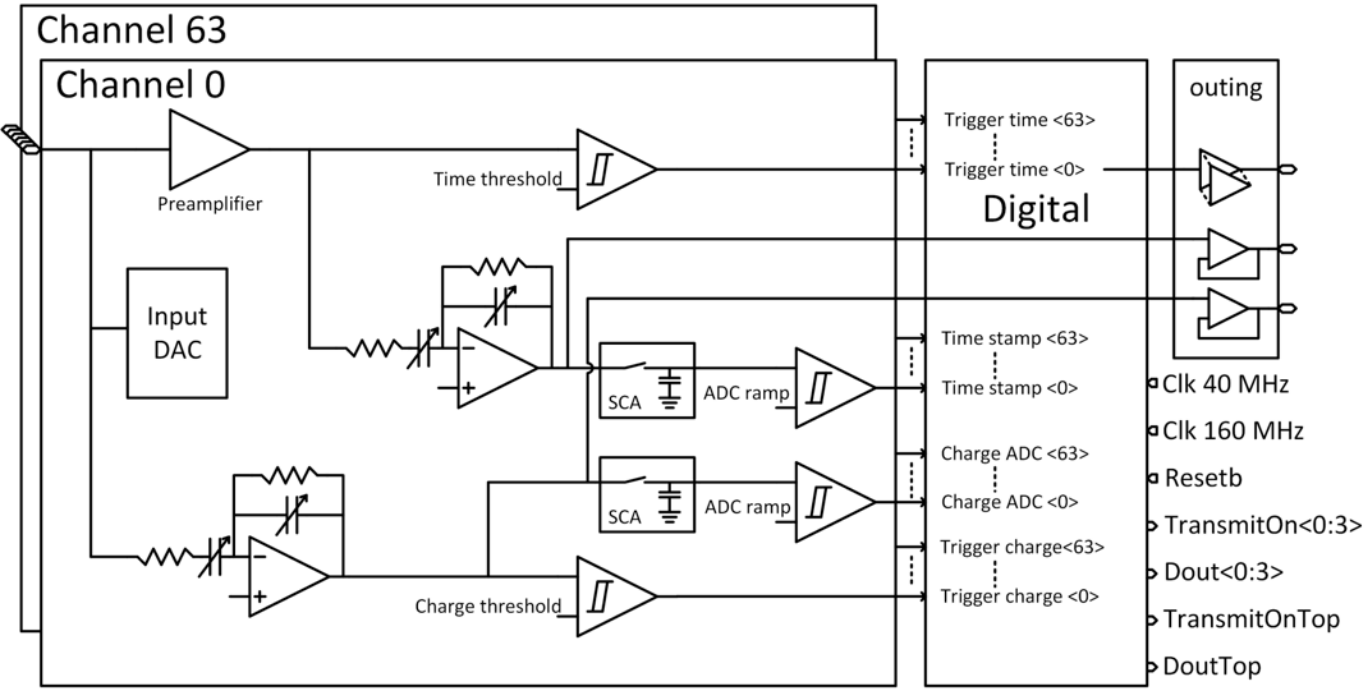
Injection (pe)	Jitter (ps)
5	146
10	85
15	46

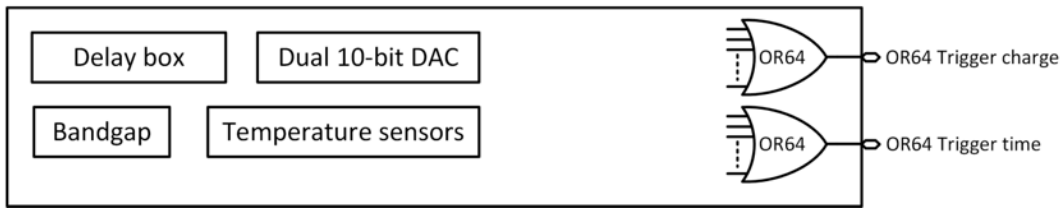


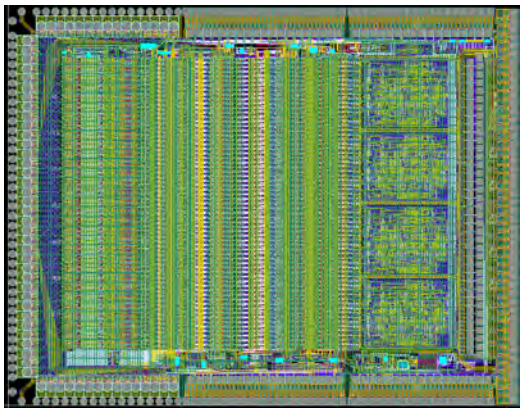
Triroc 1

- **System-on-chip** 64-channel SiPM readout : positive & negative polarity inputs
- **Trigger** : 2 thresholds/channel : timing & energy validation
- On chip ADC & TDC, zero suppress
- Power Pulsing : Analog, ADC & Digital
- Event rate : 50k events/s (minimum, driven by conversion & data outing)

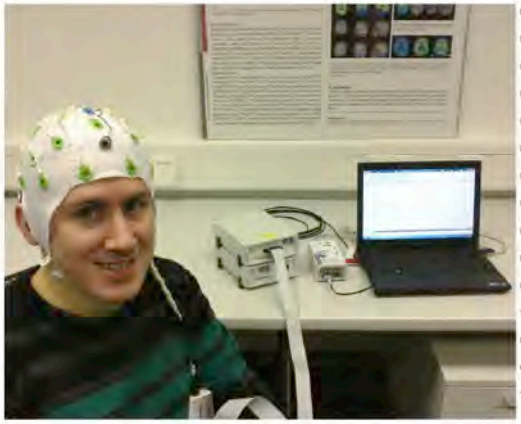
The research leading to these results has received funding from the European Union Seventh Programme under grant agreement n° 602621

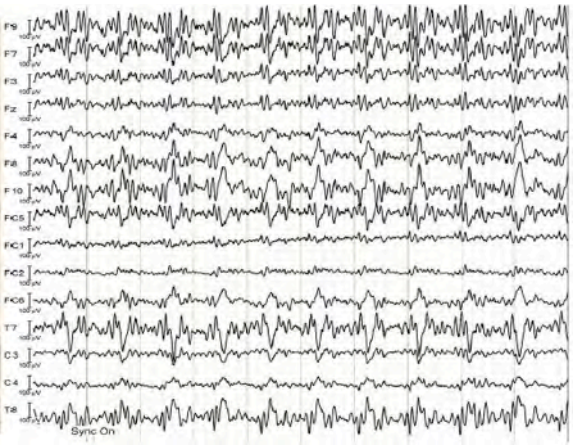


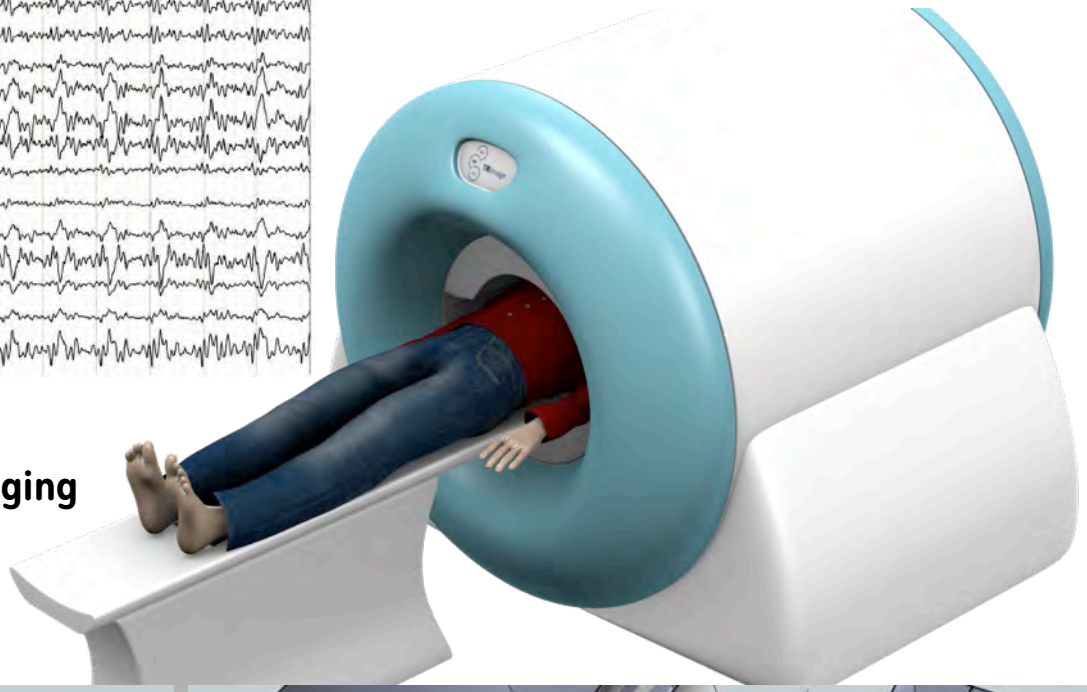




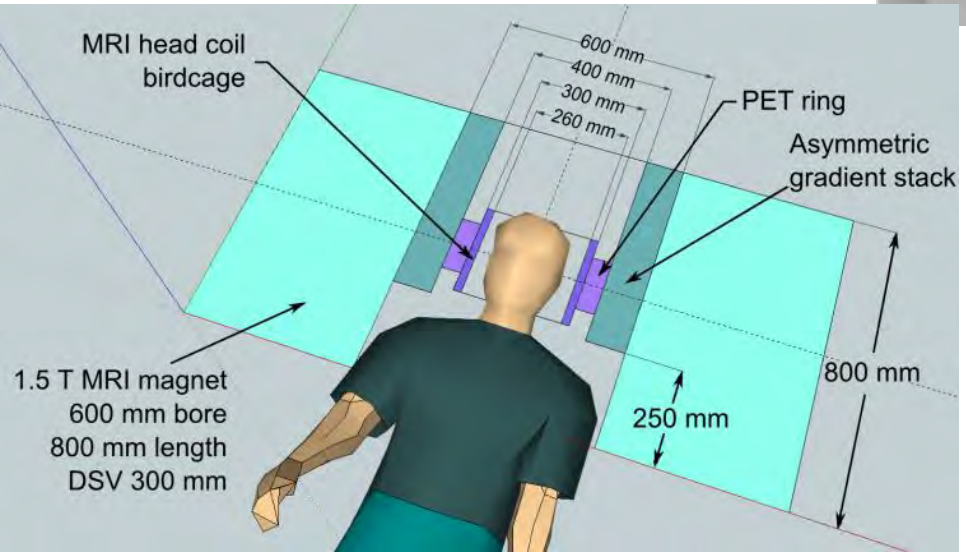
The TRIMAGE system

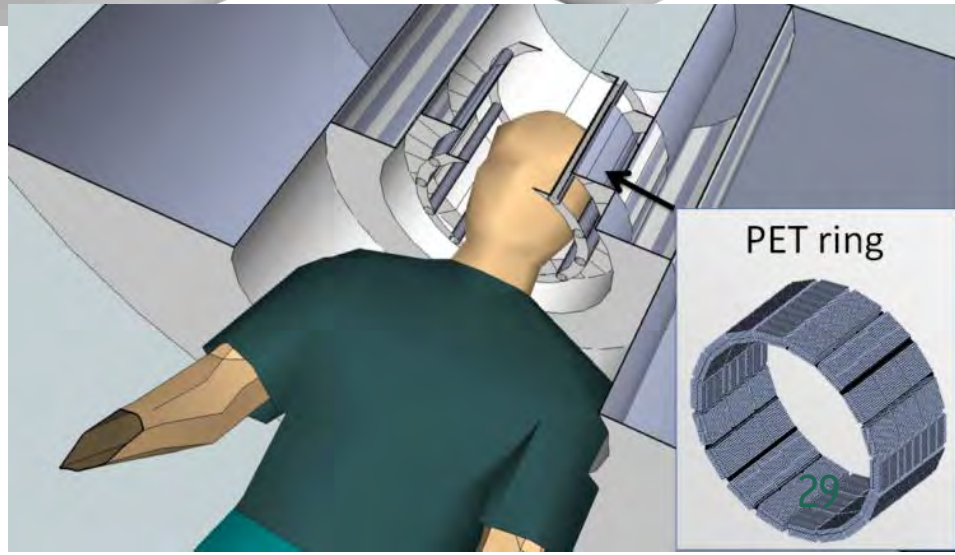






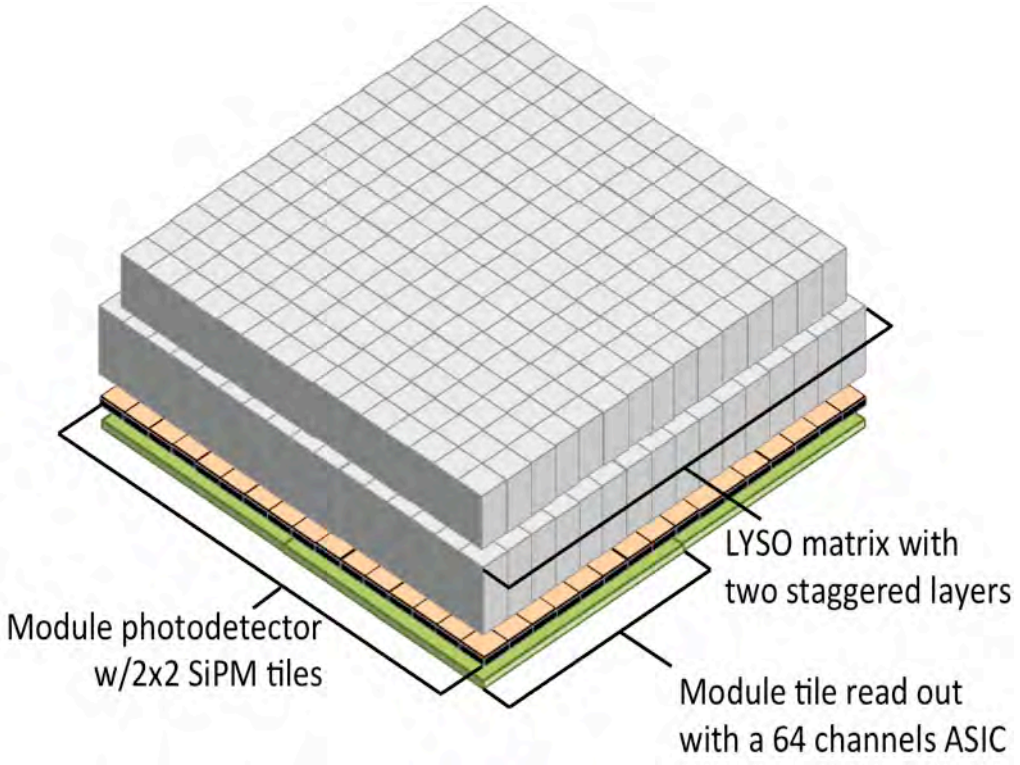
- **MRI / PET / EEG cost-effective brain imaging**
- **Schizophrenia diagnosis**



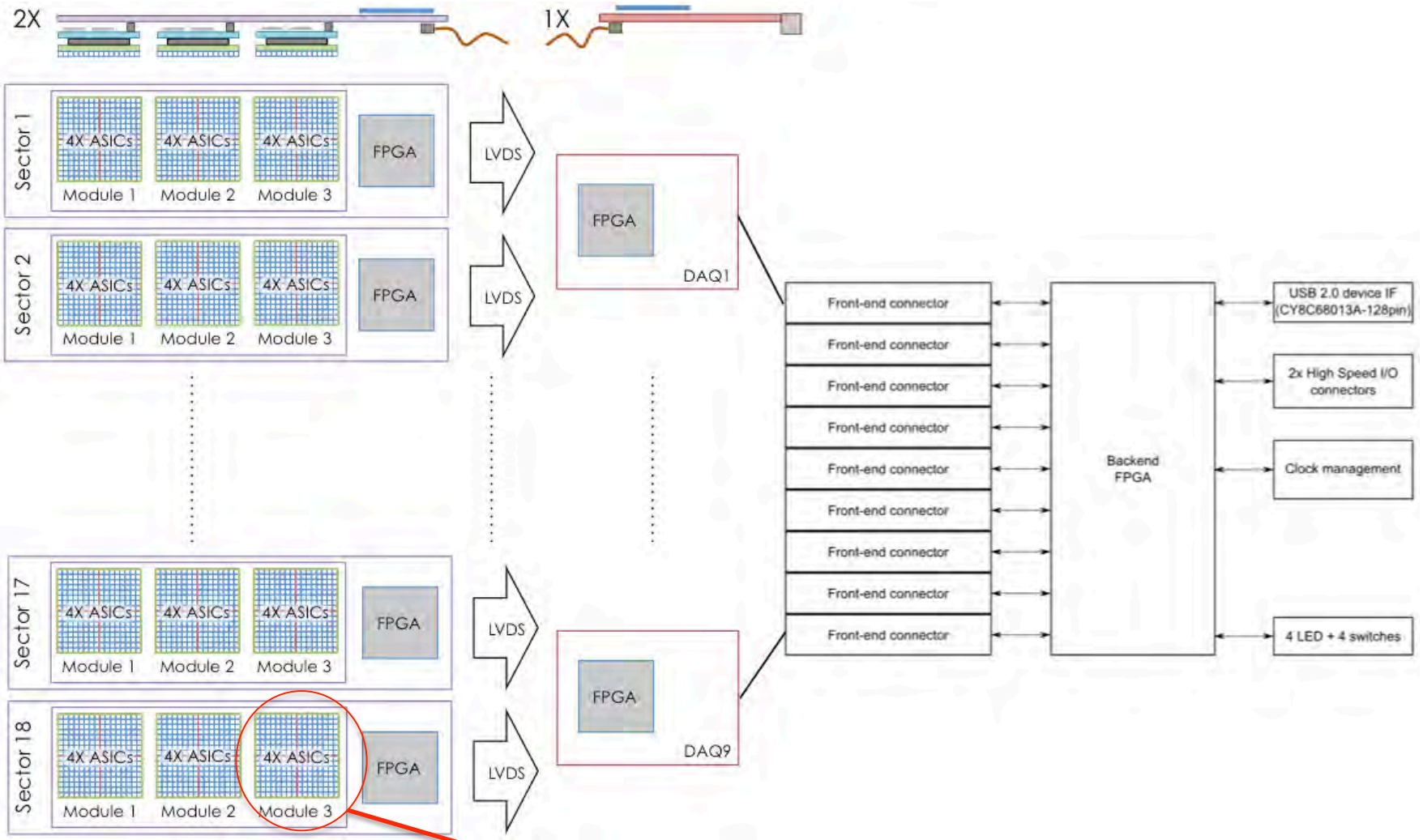


PET ring : Gamma Camera Module

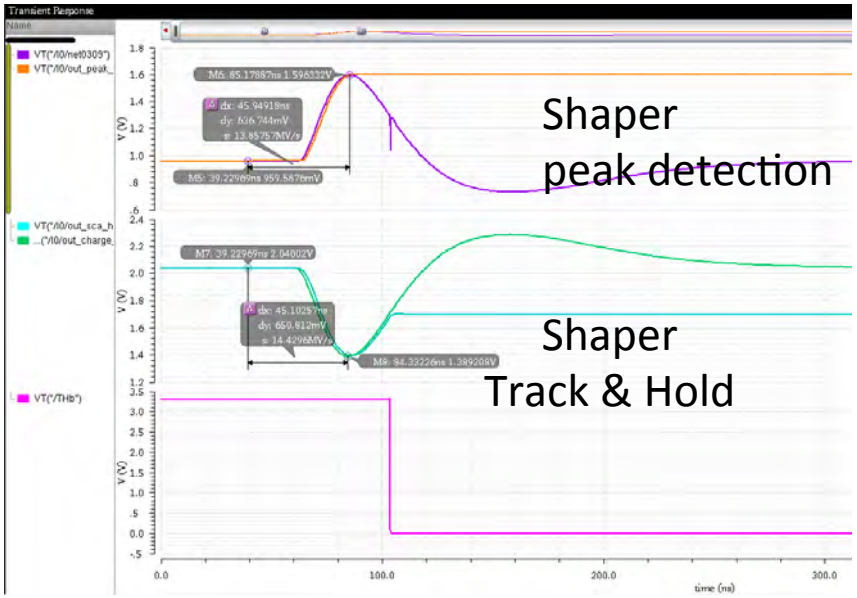
- 256 channels per module (50x50mm)
- 54 modules per ring, 14k channels
  - 64-channel ASIC, 216 ASIC per PET ring
  - Front-end board with SIPM on one side and FEE on the other side



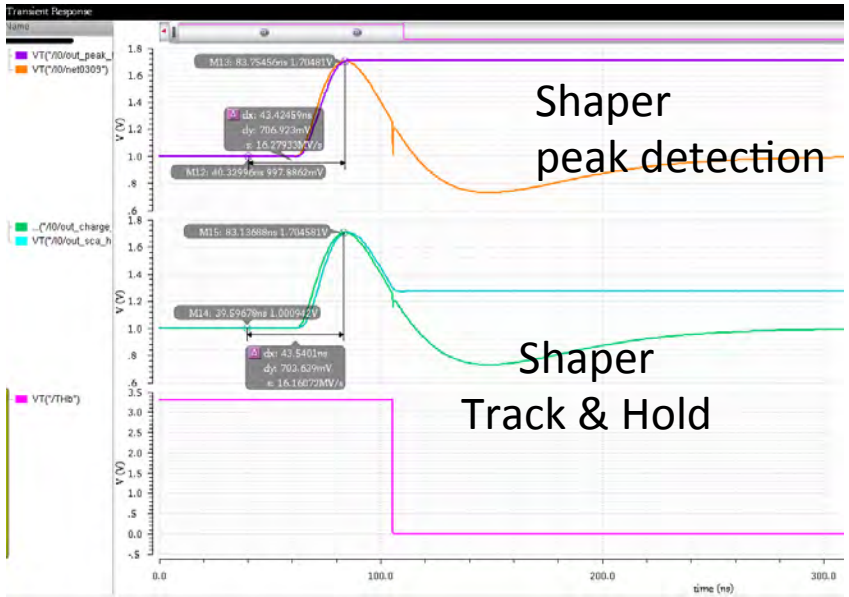
PET ring : one module



Simulations – High Gain Shaper



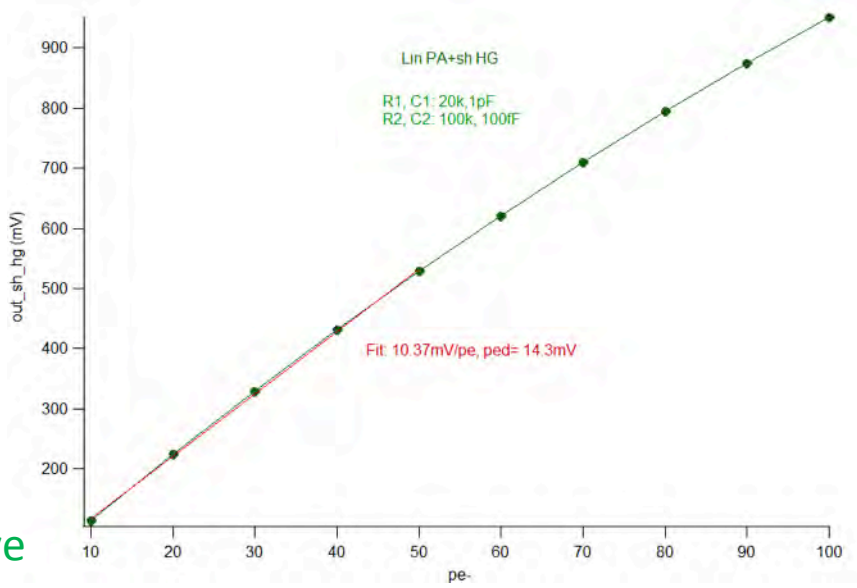
Positive input



Negative input

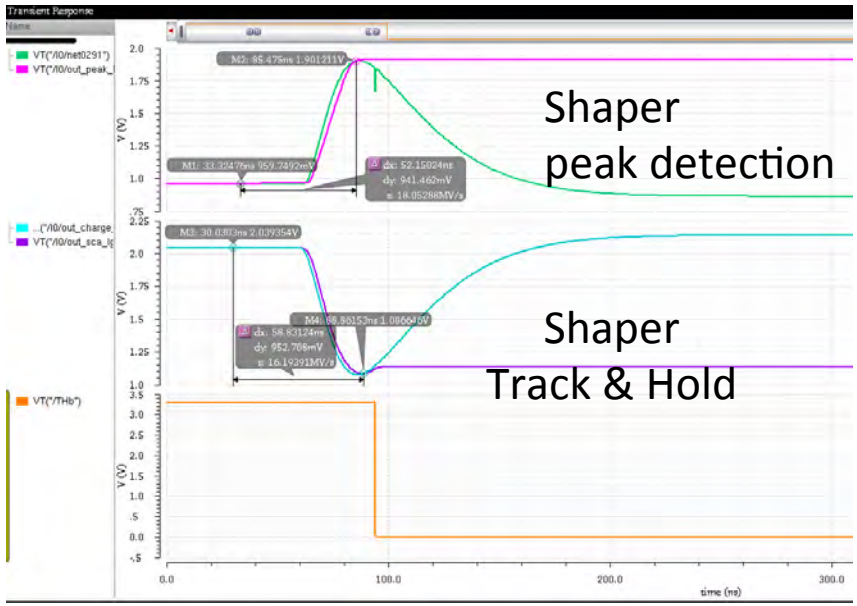
High gain Shaper simulations

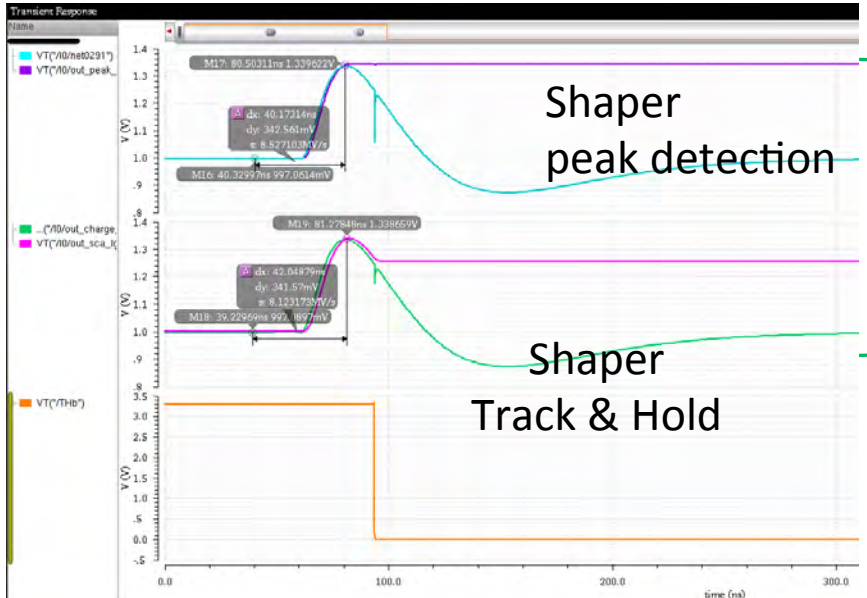
- Input charge : 20 pe
- Shaper peaking time : 10 ns



High gain shaper linearity up to 100 pe

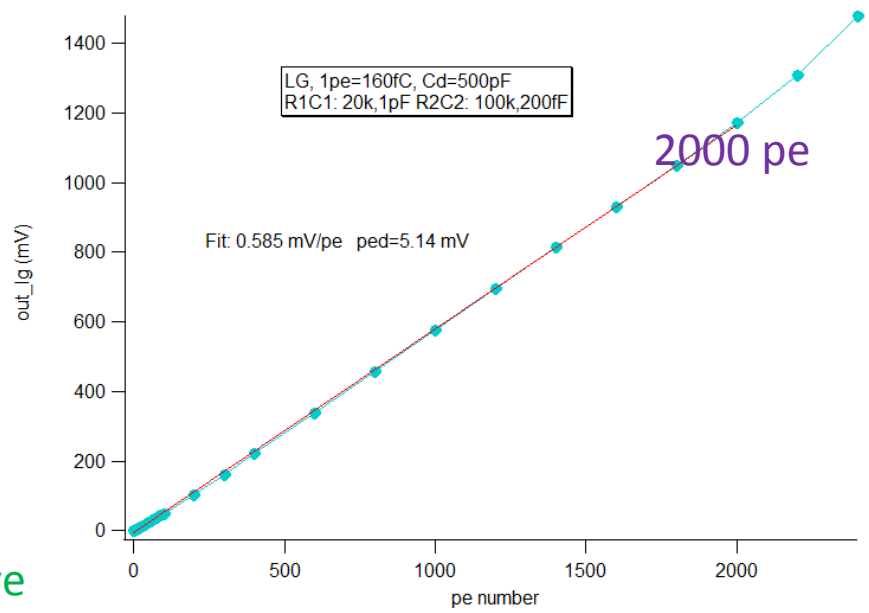
Simulations – Low Gain Shaper





Low gain Shaper simulations

- Input : 1000 pe
- Shaper peaking time : 20 ns

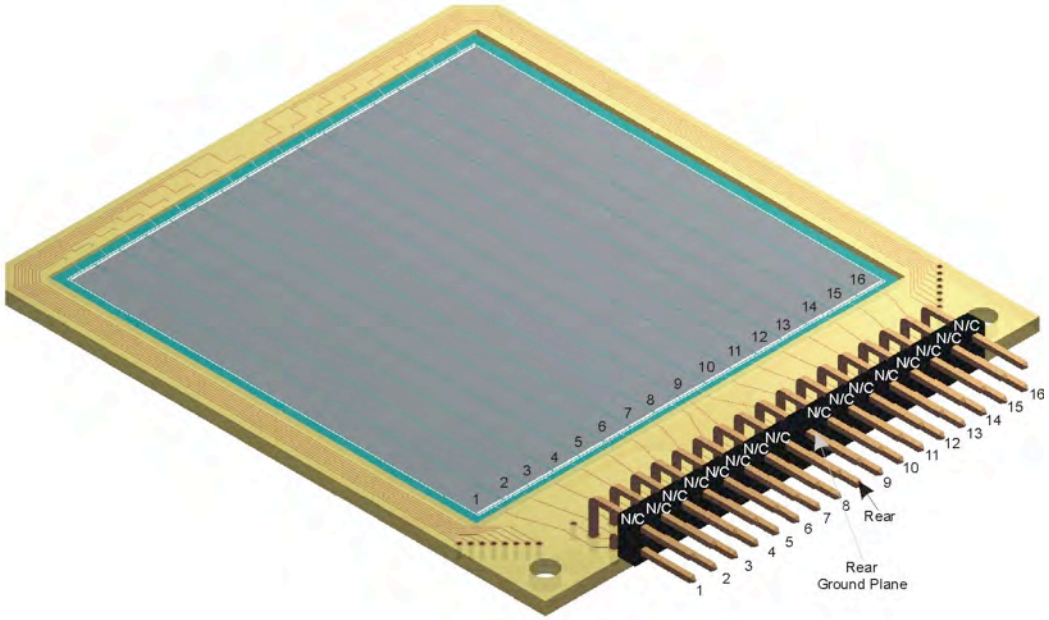


Low gain shaper linearity up to 2000 pe

Power consumption

VDD = 3.3V, without Output Buffer power consumption

- Bias + common bloc : 11.815 mA * 3.3V = 39mW
  - 1-channel : 0.6mW
- 64-channel : 125.76 mA * 3.3V = 415mW
  - 1-channel : 6.5mW
- Digital : ~16 mA *3.3V = 53mW (estimation)
  - 1-channel : 0.8mW
- Total for 1-channel : 7.9mW



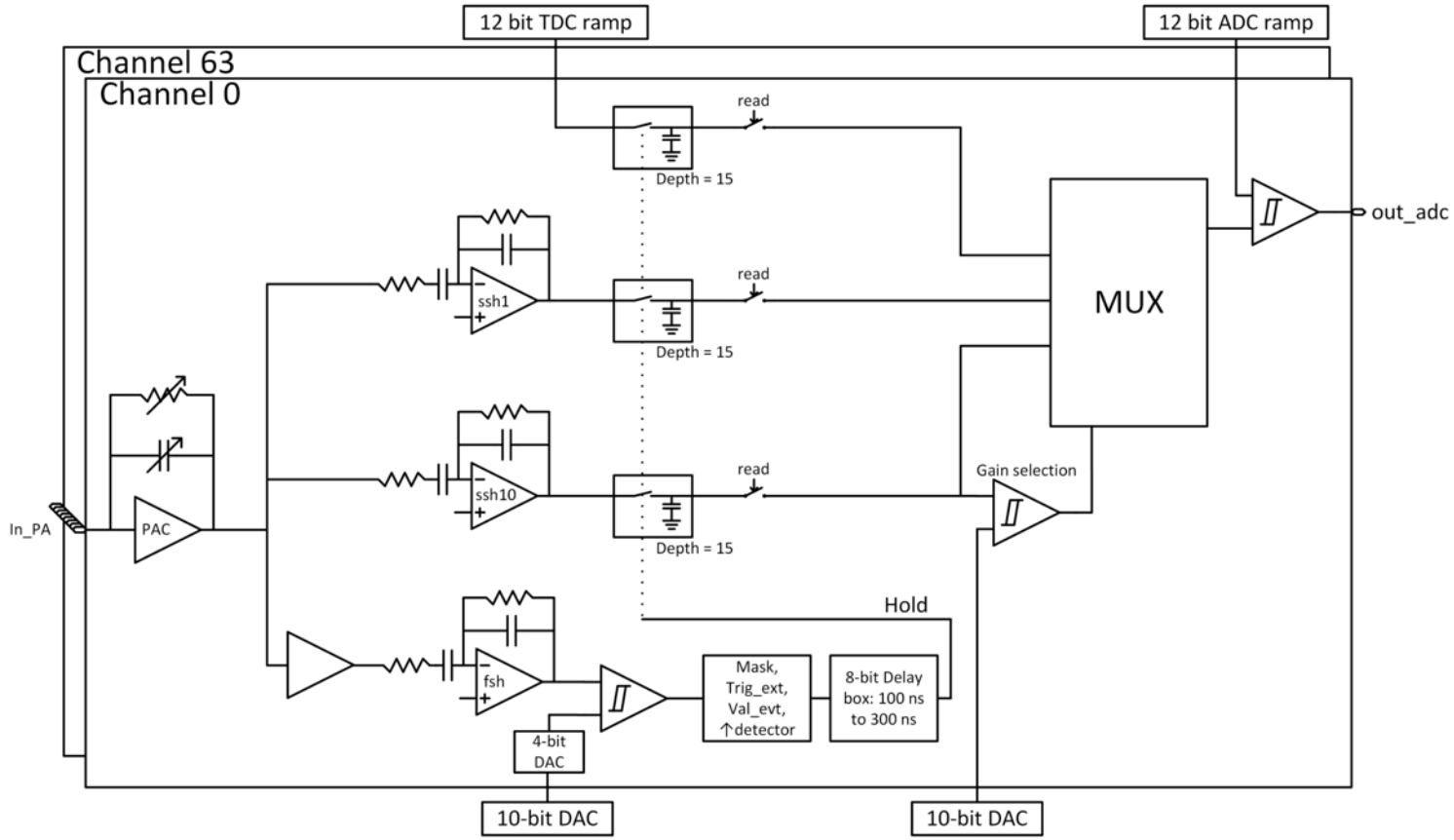
PIN DIODES – SI STRIPS

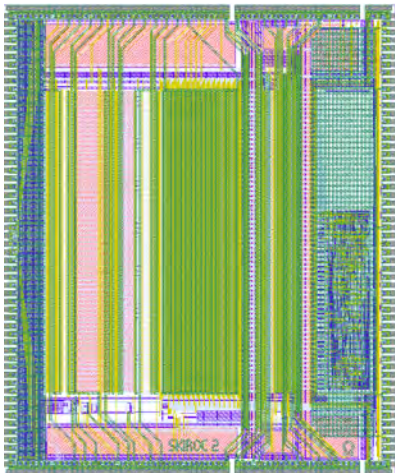
Skiroc

Skiroc 2

SKIROC2: 64 channels (W-Si ECAL, ILC, Calice collaboration)

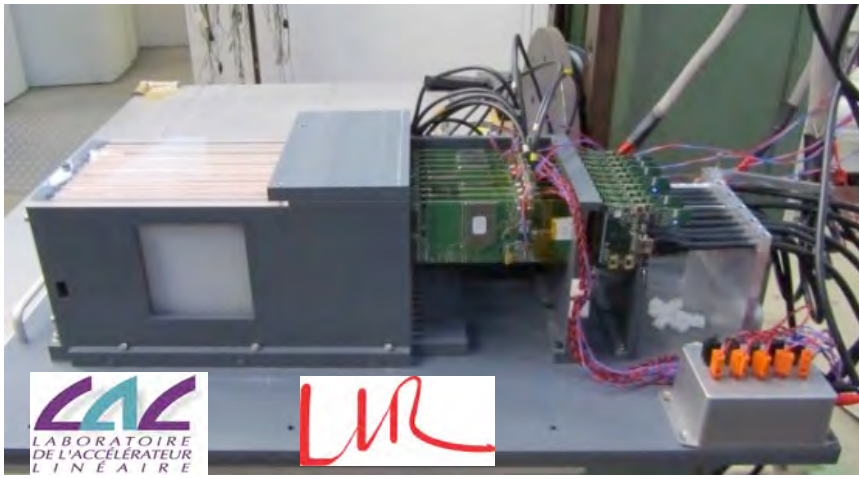
- preamp + 3 shapers + discri
- Trigger :sensitivity 0.2fC dynamic range up to 10 pC
- memory to store 15 events
- Full power pulsing, fully integrated ILC sequential readout

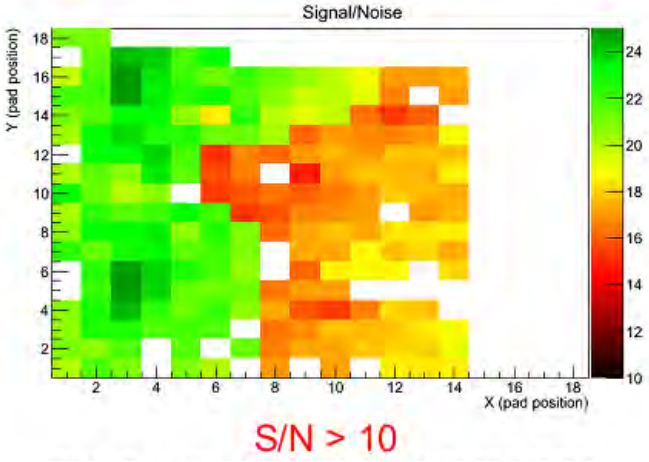


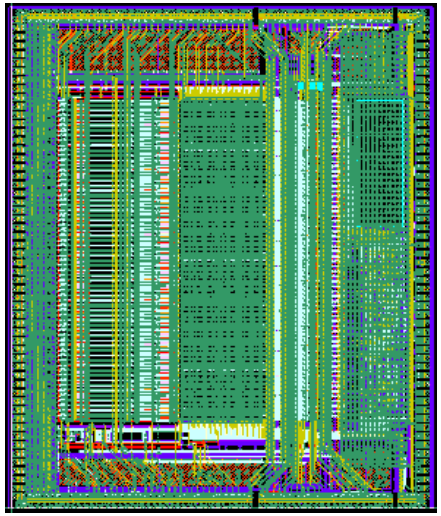


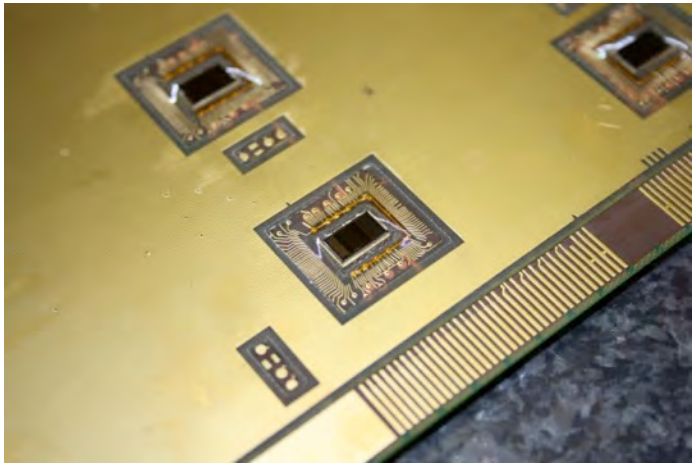
SKIROC : SiECAL chip

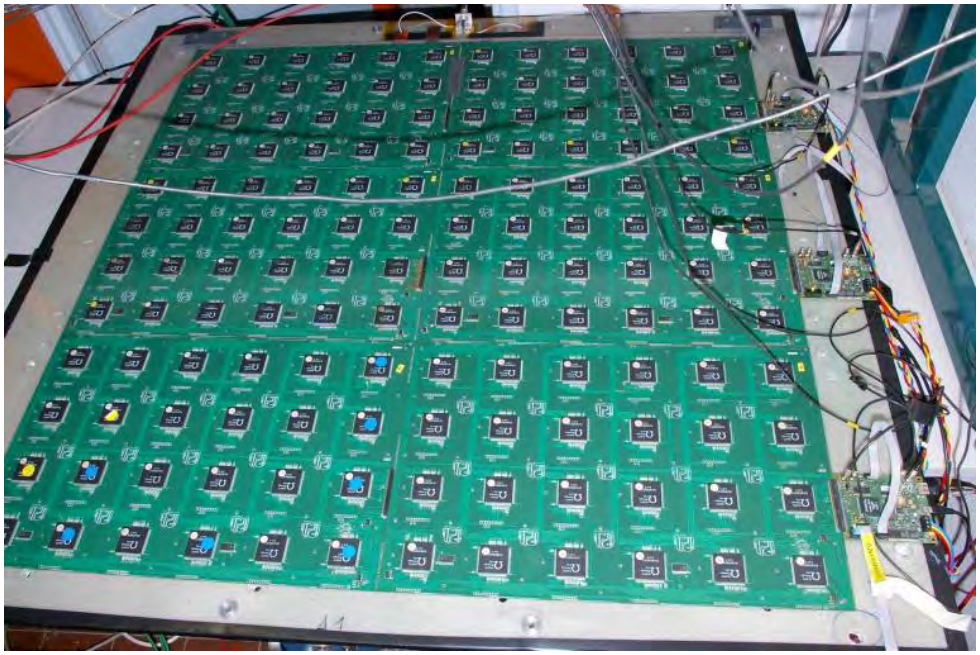
- 64 ch Si readout chip
  - Autotrigger @ · MIP = 2 fC
  - Charge measurement 15 bits
  - Time measurement







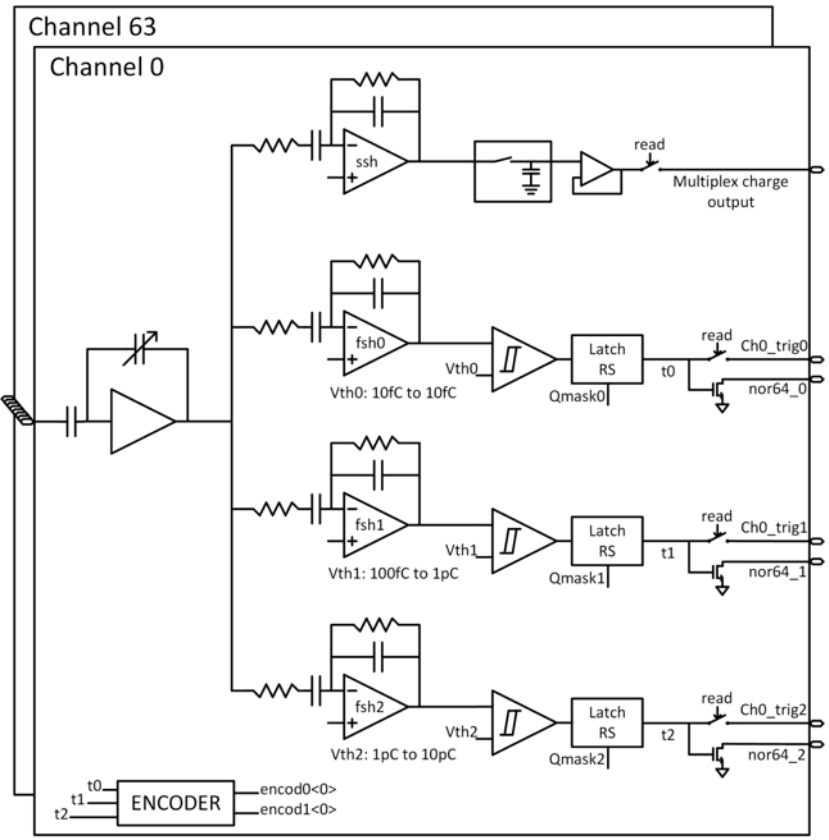


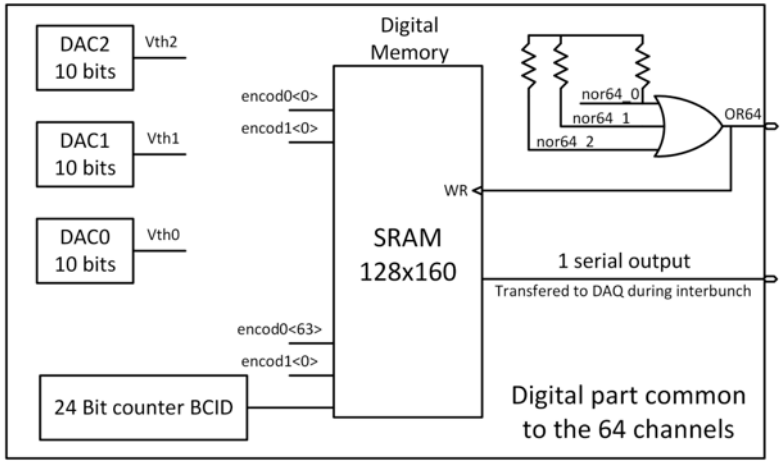


RPC – MICROMEGAS - GEMS

Hardroc, Microroc

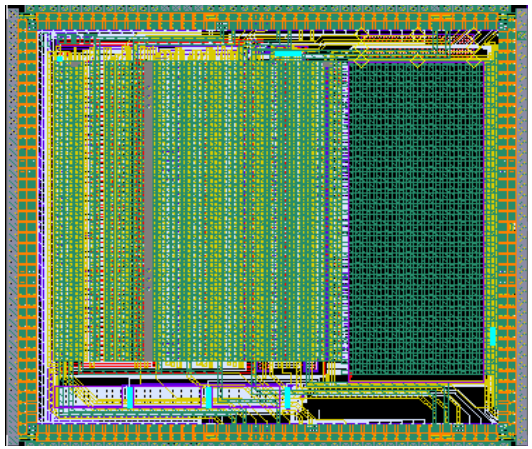
Hardroc 3



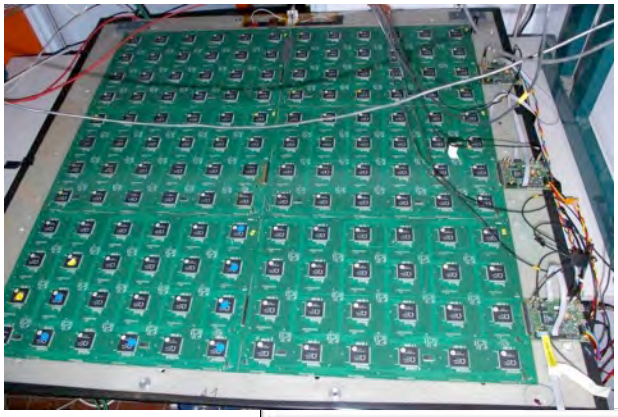


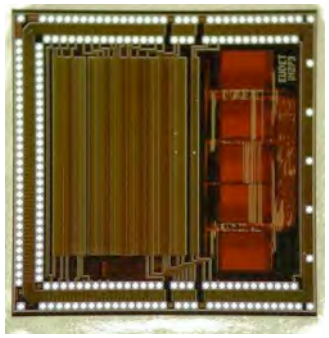
HARDROC2: 64 channels (RPC DHCAL)

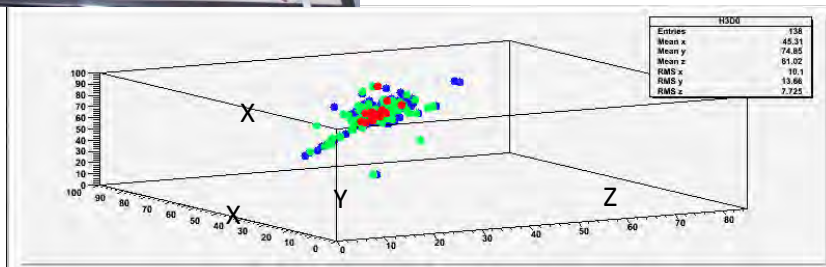
- preamp + shaper+ 3 discris (semi digital readout)
- Auto trigger on 10fC up to 20 pC
- 5 0.5 Kbytes memories to store 127 events
- Full power pulsing => 7.5 µW/ch
- Fully integrated ILC sequential readout

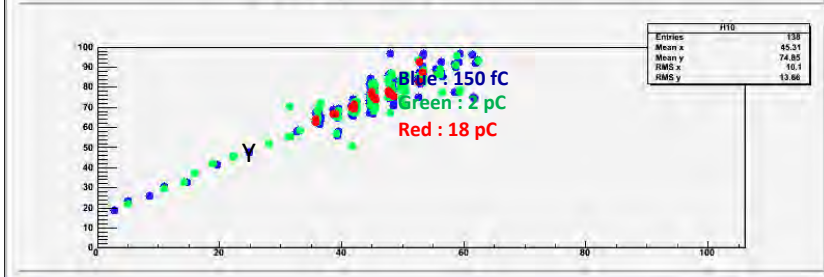


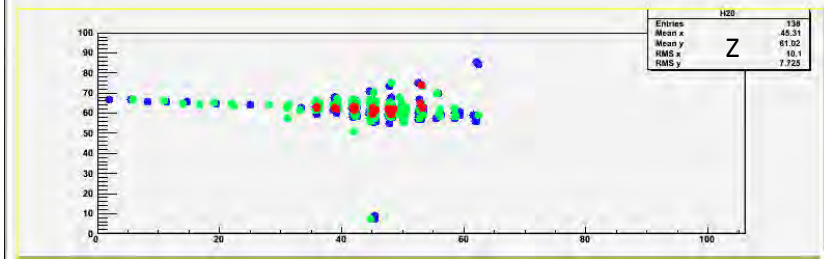
CALICE DHCAL - RPC readout











- 10 000 chips produced to equip 400 000 ch
- SDHCAL technological proto with 40 layers (5760 HR2 chips) built in 2010-2011.
- Successful TB in 2012 : 40 layers with Power Pulsing mode

lapp
Laboratoire d'Annecy-le-Vieux de Physique des Particules

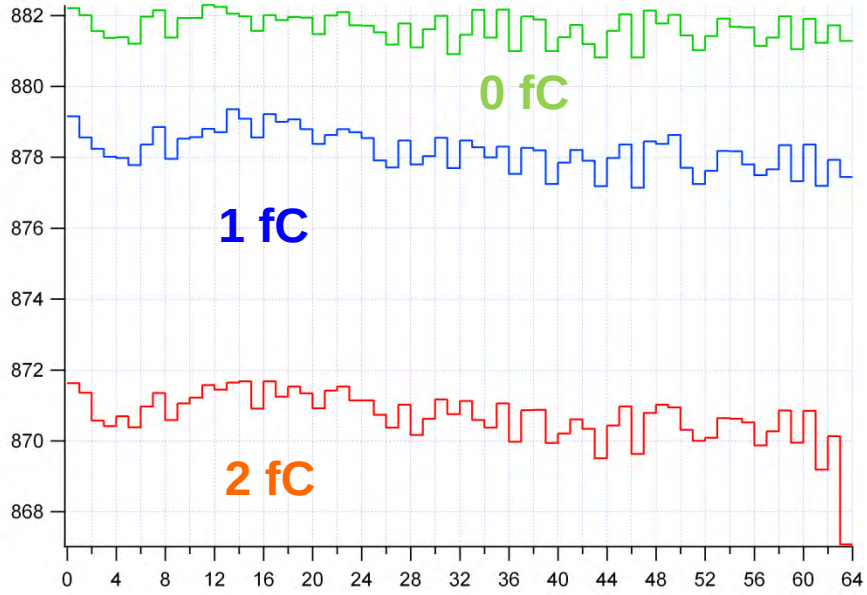
iPNL

EUDET

Variant: MICROROC

MICROROC: 64 channels for µMegas (DHCAL ILC)

- ❑ Very similar to HARDROC except for the input preamp (collaboration with LAPP Annecy) and shapers (100-150 ns)
- ❑ Noise**: 0.2fC Cd=80 pF => Auto trigger on 1fC** up to 500fC
- ❑ Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- ❑ **HV sparks protection**
- ❑ 1 m2 in TB in August and October 2011. Very good performance of the electronics and detector (Threshold set to 1fC).
- ❑ 2012: 4 m2 in TB

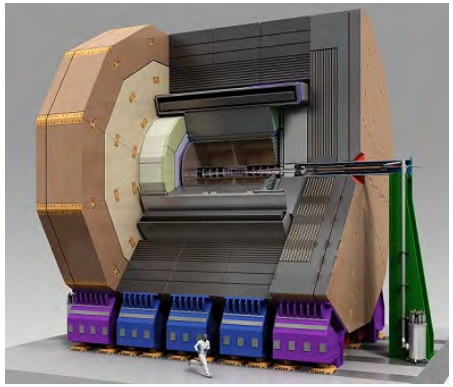


@LAPP Annecy

1m2 equipped with 144 MICROROC

ROC chips for ILC detectors

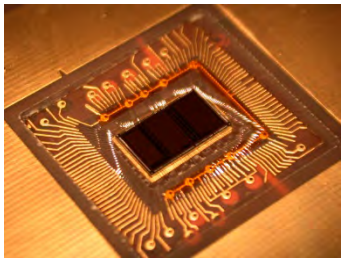
Imaging calorimetry at the International Linear Collider



⇒ New detectors with one hundred million channels

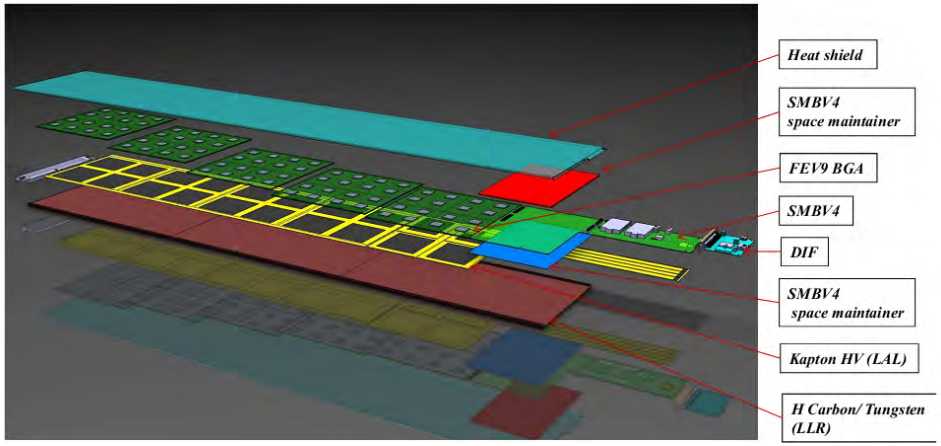
⇒ Readout electronics:

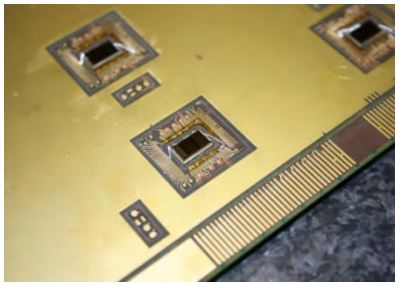
- Large dynamic range (15 bits), auto-trigger on ½ MIP
- must be highly integrated (System On Chip) and ultra low power to be embedded inside the detectors



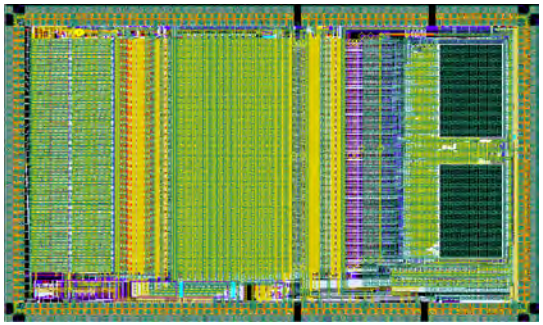
⇒ Readout ASICs: HARDROC, MICROROC, SPIROC and SKIROC in SiGe 350 nm technology (AMS) by OMEGA

http://omega.in2p3.fr/



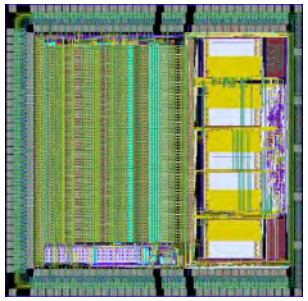


ILC CALICE collaboration : read-out framework

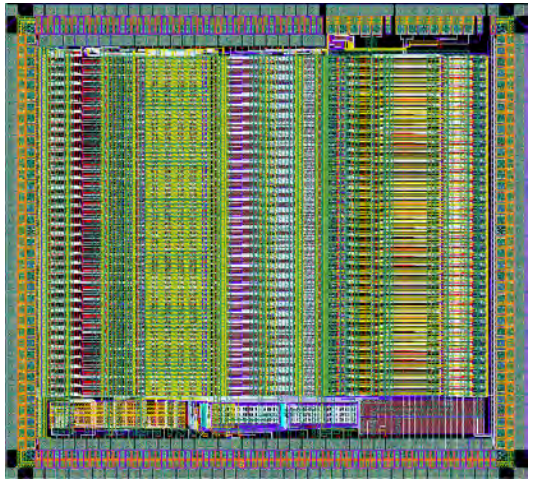


SPIROC
Analog H-CAL
(SiPM)
36 ch. 32mm²

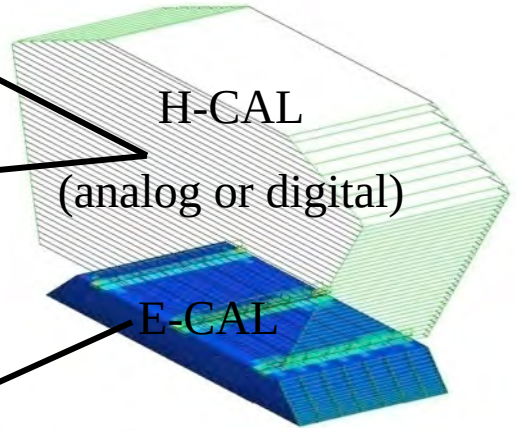
- Technological prototypes : full scale modules (~2m)
- ASIC designed within the CALICE collaboration and EUDET (EU funding 2006-2010)
- ECAL, AHCAL, DHCAL

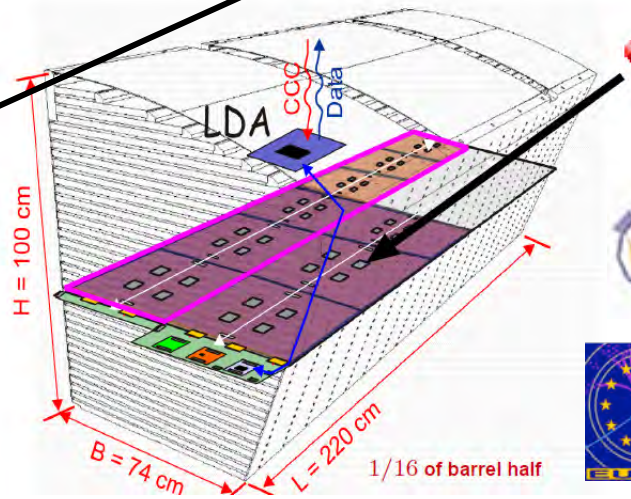


HARDROC
Digital H-CAL
(RPC)
64 ch. 16mm²



SKIROC
SiW E-CAL
(Si-PIN diode)
64 ch. 60mm²

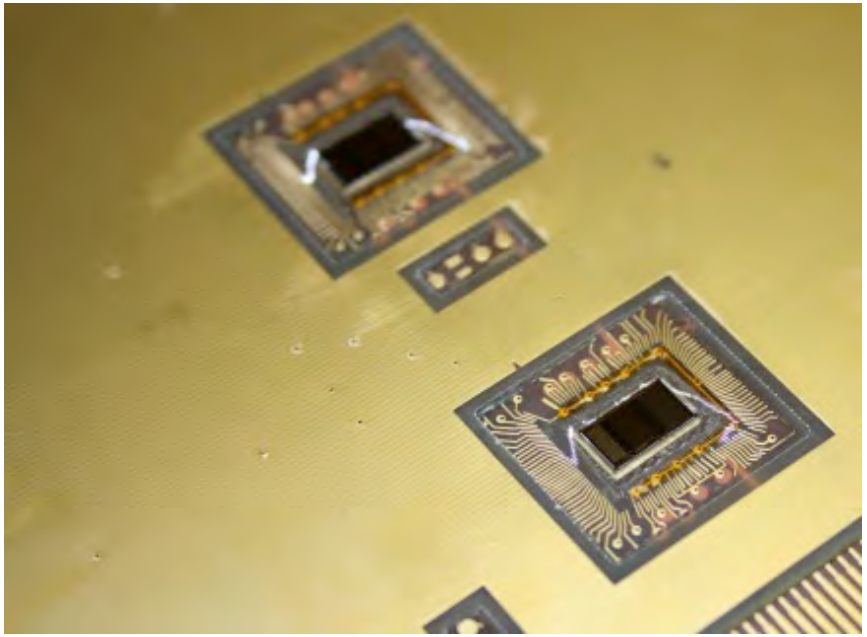


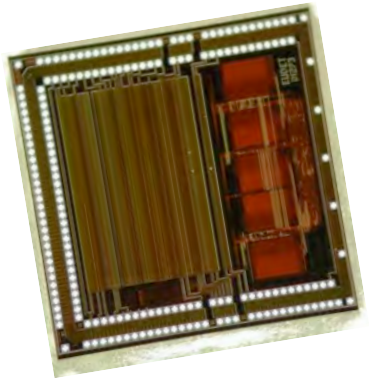


SPIROC chip:
handles signal from 36 SiPM

AIDA

CALICE Calorimeter for ILC





SUMMARY

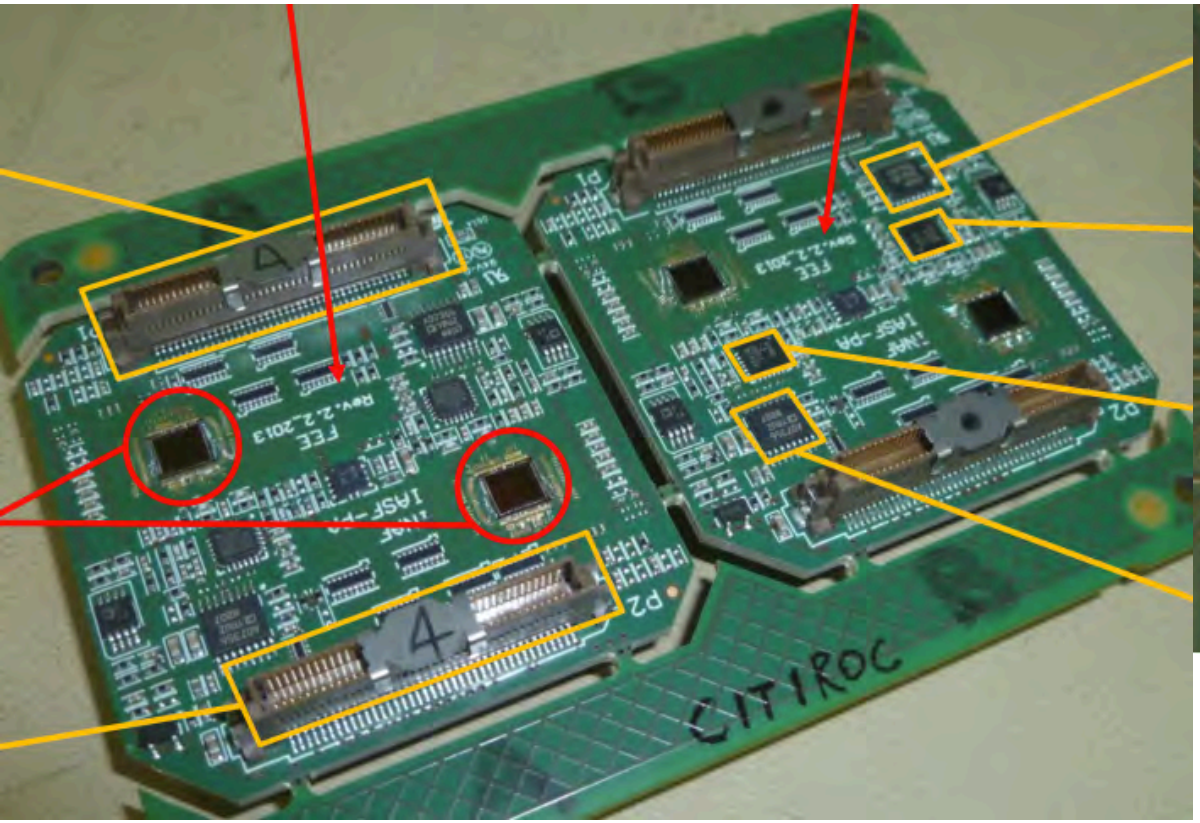
About the ROC chip in general

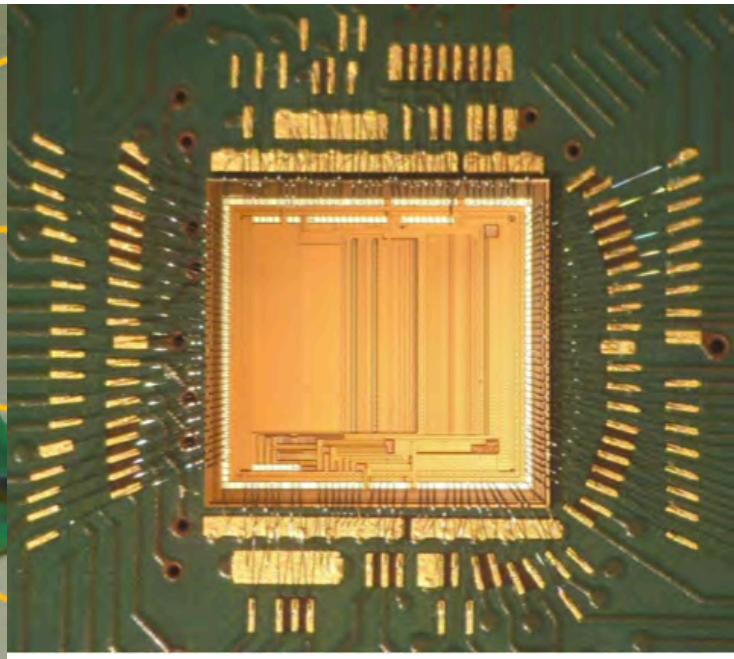
- Power effective
  - Between 1 mW and 8 mW/channel
  - Power pulsing (power down to 7.5uW/channel)

  →Low power is mandatory for large experiment (no « leakless » cooling anymore
- Complex yet comprehensive
  - Probe bus for debug and better understanding of the fine effects
- Versatile
  - All ASICs are programmable (gain, peaking time, threshold)
- Two trends
  - « simpler » front-end ASICs with many I/Os (analogue outputs, all trigger out)
  - System-on-Chip for highly integrated systems

Packaging

- Less naked die, less TQFP, more BGA
  - Wire bonding is not cost effective and complex to handle
  - TQFP are convenient but to big
  - Fine pitch BGA are very promising (ex. Citiroc in 10x10x1.2mm BGA)





ROC chip family at a glance

Chip	Detector	Ch	Polarity	Dyn Range	Specificities
MAROC	PM	64	<0	5 fC - 5 pC	64 trig outputs, internal 8/10/12-bit ADC (for charge measurment)
SPACIROC	PM	64	<0	2 pC- 220 pC	Fast photon counting (50MHz)
PARISROC	PM	16	<0	5 fC - 1 pC	Internal TDC (<1ns), 16 trig outputs
HARDROC	RPC	64	<0	2 fC - 10 pC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
MICROROC	µMEGAS/GEM	64	<0	0.2 fC - 500 fC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
SKIROC	Si pin diodes	64	>0	0.3 f C - 10 pC	Internal 12-bit ADC for charge measurement
SPIROC	SiPM	36	>0	10 fC - 300 pC	36 HV SiPM tuning (8 bits), Internal 12-bit ADC for charge and time measurement
EASIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	Both	100fC – 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)
TRIROC	SiPM	64	Both	100 fC- 300 pC	64 HV SiPM tuning (8 bits), 64 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)

Thank you